28. QCA Adder-Subtractor

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ABSTRACT

Quantum-dot cellular automata (QCA) is one of the promising emerging technologies being investigated as an alternative to CMOS technology. This paper investigate the suitable design for optimized one-bit full adder (FA) for implementation in QCA. Also the fault tolerance of the proposed FA outputs due to the missing cell defects are analyzed, and the test vectors for detection of all expected faults are identified. QCADesigner software is used for design and simulation. The proposed designs are compared with previous works. In comparison with the compared previous design, the proposed FA has 25% and 26% improvement in cells count and area, respectively, and it is faster. For the proposed FA, the obtained results ascertain that these designs are more efficient in terms of area, cell count and delay. Therefore, the implementation of proposed designs may be used as a basic building block of a nanoprocessor.

Keywords— *Quantum-dot cellular automata, QCA, QCADesigner, majority gate, full adder.*

INTRODUCTION

Current CMOS technology has scaled down to few nanometer technologies. Present silicon CMOS technology is facing exigent problems, such as quantum mechanical effects, high power dissipation and profound problem in feature size reduction. We must go for altered structure of CMOS or alternate of CMOS, and nanotechnology is an answer to these problems. The international technology roadmap for semiconductors (ITRS) report [1] presents various possible technology solutions. Quantum-dot cellular automata (QCA) [2–5] is a nanotechnology that offers a promising method of computation, Signal processing and Signal transformation. Full adder (FA) Presents one of the most important building block of arithmetic and digital circuit. Designing a fast and smaller full adder is indispensable. Many researches has been targeted upon the implementation of adders with QCA technology [7–10]. Optimized design of one bit FA where carry is used as one of the input for implementation of sum is implementation in QCA has been presented here. Simulation of missing cell defects have been done and identification of test vectors for the detection of missing cell faults for the proposed one bit FA have been presented here. Comparison of the proposed FA with previous designs [7–10] have been done. Results ascertain that the proposed design is more efficient in terms of cell count and effective area in comparison with the other works referred. Further, reduction in number of clock phases, shows extremely low delay may be obtained using an optimized layout.

BASIC QCA CIRCUITS

Figure 28-1 gives schematic of the ideal QCA cell structures in ground state, which have four identical QDs represented as open circles, forming corners of a square. Two electrons are assumed, represented by solid dots, in each cell occupying the diagonal positions. The polarization is defined as given in figures 1(a) and (b), anticlockwise position to be -1 polarization (P = -1) and clockwise position to be +1 polarization (P = +1) respectively.

In a cell the electrons are allowed to jump between the individual QDs using quantum mechanical tunnelling. In an isolated cell the electron will occupy the diagonal dots at ground state due to the coulombic force possessing either of polarization. This gives a bistable latch like behaviour with only two stable states. The nearby cells have

sufficient barrier in form of intercellular distance, to completely suppress the tunnelling to occur between adjacent cells. Coupling between two adjacent cells is governed by the coulombic interaction and clocking action. Figure 28-2 shows the coupling between the adjacent cells, which compels cell 2 to have the same polarization as cell 1.

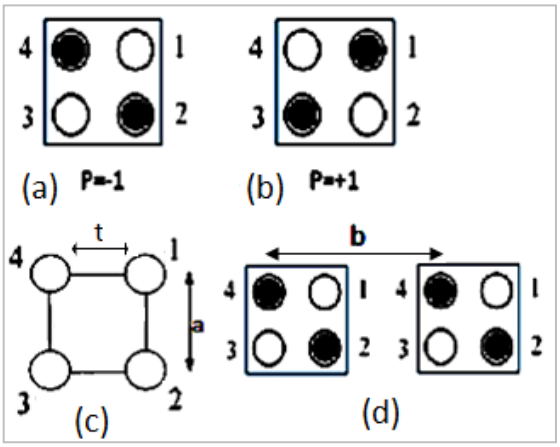


Figure 28-1 Ideal QCA cells, with (a) -1 polarization (b) +1 polarization, (c) dimensions of the cell (d) intercellular distance

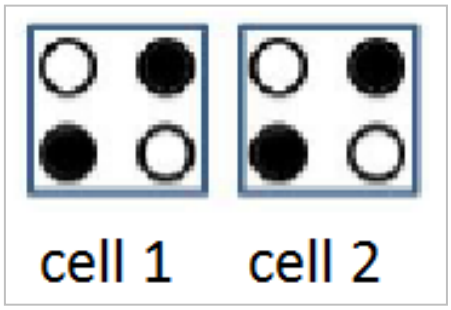
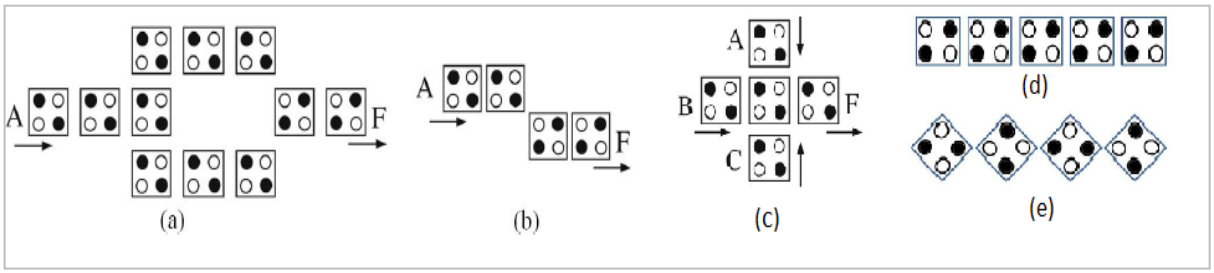


Figure 28-2 Cell 2 has the same polarization as cell 1 due to coulombic interaction.

The physical interaction between cells may be used to realize elementary Boolean functions. The basic logic gates using QCA structure are given in figure 28-3.



Figur 28-3 (a) Redundant inverter gate, (b) Inverter gate, (c) Majority logic gate, (d) Binary wire and (e) Inverter chain

Majority logic function given in figure 28-3(c) is the most important logic gate, with which we can implement OR gate when one input is permanently fixed to logic 1, and AND gate can be implemented fixing one input to logic 0. Clocking is very important aspect of QCA, which not only provides a mean for synchronizing information flow along the circuit, but also controls the direction of information flow in a QCA circuit. The QCA clock also provides the power required for the logic operations. Actually, the clock is used to control the tunnelling barrier height of QD in a QCA cell. Clocking scheme can be divided into four regions as given in figure 28-4(a). When clock gets low, the electron gets trapped in QD and cannot tunnel to other QD. This is the hold phase. When the clock signal is high, all QD's barrier gets lower and electrons are free to move. This may be called to be null polarization state or relax phase.

Figure 4(b) shows QCA clock, each cell in a particular clocking zone is connected to one of the four available phases of the QCA clock. Each cell in the particular clock zone is latched unlatched, and synchronized with the changing clock signal.

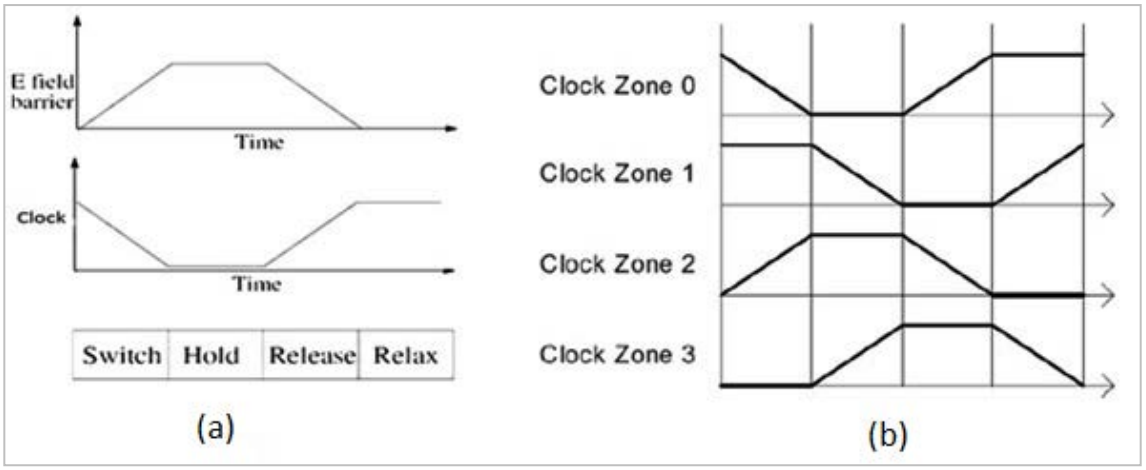


Figure 28-4 (a) Clocking scheme, clock regions and corresponding barrier potential, (b) QCA clock Zone

PROPOSED DESIGN

The equations for a FA realized with majority gates and inverters are given by:

$$S = a.b.cin + a.\bar{b}.\overline{c_{in}} + a.\bar{b}.\overline{c_{in}} + a.\bar{b}.\overline{c_{in}} = M(\bar{M}(a,b,c_{in}), M(a,b,\overline{c_{in}}), c_{in}) \quad \text{.....(1)}$$

And

$$c_{out} = M(a,b,c_{in}) \quad \text{.....(2)}$$

The schematic diagram of one-bit FA is presented in Figure 28-5. Main improvement lies in the use of carry output for implementation of sum. Design of logical structures using two inverters has been proposed. With the application of this method, the number of QCA cells has been reduced. Moreover designing two layers with a part of the calculation in layer 2 have been done in order to obtain the outputs, create the presented layout an effective design with the profound reduction in number of cells, with small size and minimum delay. Using this method the layout of the proposed single bit FA is obtained as given in figure 6. This design is designed with two layers. And multilayer wire crossing system for crossover wires have been done. The output signals can be used as the inputs of the other QCA circuits, as it is shown in Figure 28-6. Also as the output is not surrounded by the other cells therefore it can be accessed easily. Hence, this structure does not need wire crossover to transfer output signals.

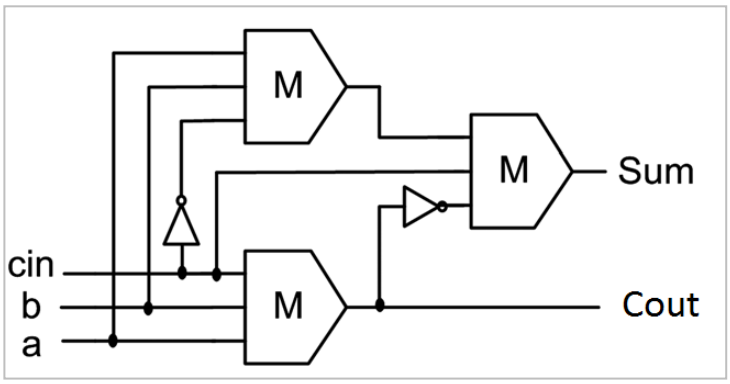


Figure 28-5 chematic diagram of the one-bit FA.

For the proposed circuit layout and functionality checking QCADesigner version 2.0.3 [6] is used. Following parameters for a coherence vector engine [6] is used: radius of effect 75 nm, relative permittivity 12.8, layer separation 11.4 nm, temperature 1° K, relaxation time 1.1 fs, time step 0.11 fs, total simulation time 72 ps, clock

high 9.8×10^{-22} J, clock low 3.8×10^{-23} J, clock shift 0, clock amplitude factor 2. Also cells are assumed to have a width and height of 20 nm, and quantum dots have 5-nm diameter.

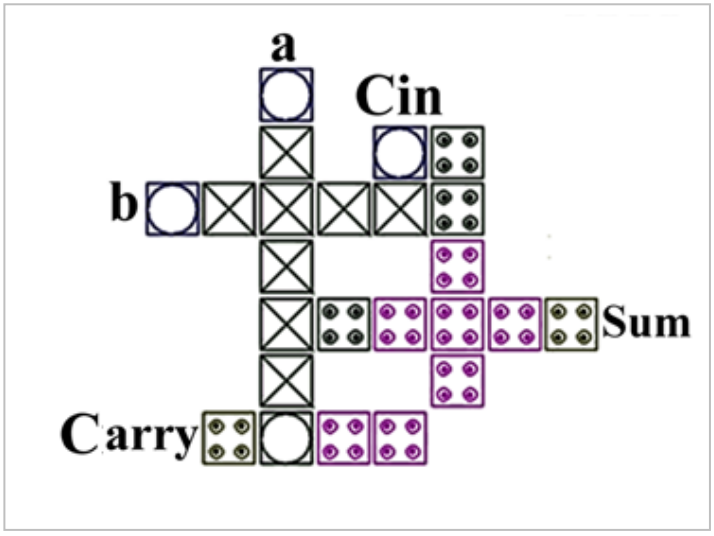


Figure 28-6 Layout of one-bit FA.

FAULT TOLERANCE IN THE PROPOSED FULL ADDER

Recently, fault-tolerant properties and characteristics of QCA for is the buzz word and have been reported by many researchers [7-9]. The cell misplacement, cell misalignment cell missing cell, misshapen cell, and additional cell defects are the identified defects as well as single electron fault, three electron fault etc as identified as faults in QCA circuits [11-13]. Here, simulation of missing cell defects and identification of the test vectors for detection of all faults for the proposed FA are provided. For all simulations, a particular cell labelled with the number i, shown in Figure 6, is deleted in the original (defect-free) configuration of the proposed FA. The new configuration has been simulated using QCADesigner with its coherence vector engine. The simulation results show that deleting the cells with the numbers 1 to 16 results desired output in output Carry; also deleting the cells with the numbers 5, 28, 30 and 31 results desired output in output Sum. In addition, for the input set {a b cin} = {000, 001, 010, 011, 100, 101, 110, 111} all distinct faulty outputs in the output Sum are obtained: {10101010, 01001101, 00010111, 01110001, 00001111, 11001100, 11010100, 01010101, 00101011, 00110011}; also, all distinct faulty outputs in output Carry are obtained: {00001111, 01001101, 11101000, 00110011, 10001110}. For detecting the effects of these defects, a test sequence can be utilized as: {a b cin} = {010, 011, 101, 110}. This test vector can detect any cell missing defects in the proposed FA layout.

RESULTS AND DISCUSSION

Waveforms of input and output signals, for the proposed one-bit FA have been shown in Figure 28-7. A detailed comparison between the proposed designs and previous works have been shown in Table 28-1, where BKA stand for Brent–Kung adder. As it is seen from Table I, in comparison with the best previous FA presented in [5,14], the important enhancements achieved for the proposed FA are 26% in the area, 25% in the cells count and 15% in the wasted area in cells, where the important improvement is obtained by the following equation:

$$\text{Important improvement} = (1-X/Y)*100 \quad (3)$$

where X is the cell count for our designs and Y is the cell count for previous designs. Also our FA is faster than the compared designs.

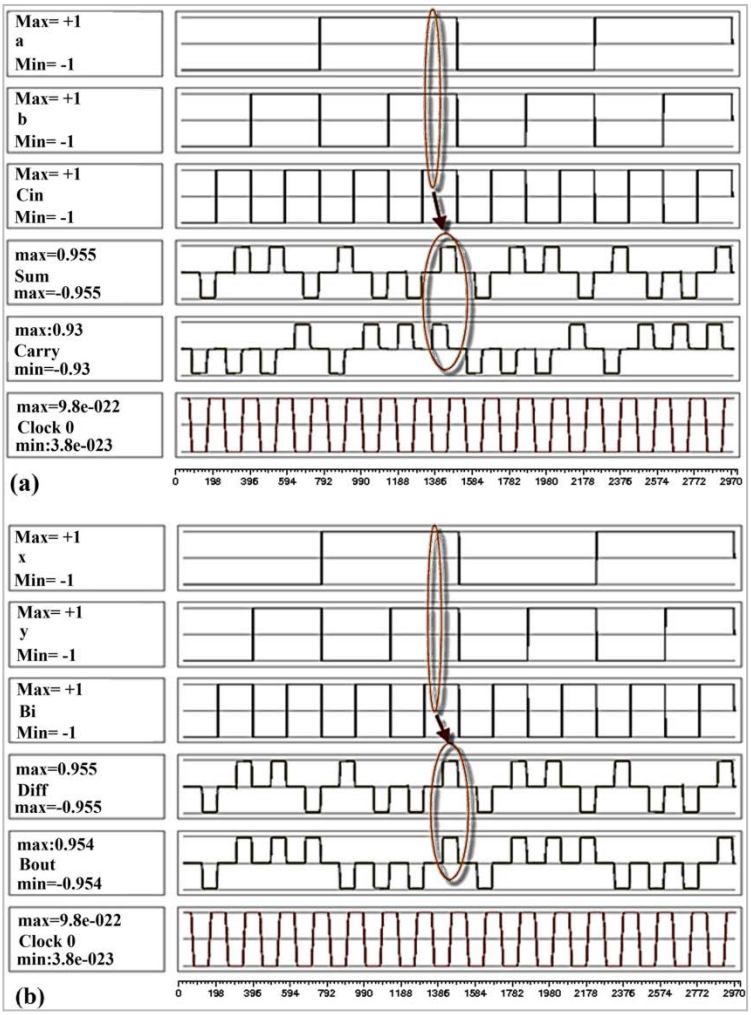


Figure 28-7 Simulation results for the proposed one-bit FA.

Table 28-1 Comparison with previous designs.

Reference	Approximate Area (μm^2)	Approximate wasted area in cells	Cell count	Delay (Clock Pulse)
Type 1[5]	0.05	84	79	5
Type 2[5]	0.03	42	51	3
Proposed FA	0.022	35	38	2

CONCLUSION

Optimized design of single bit full adder is presented in this paper. Also investigation of missing cell defect its characterization and finding the test vector to ascertain tolerant design of presented FA has been done. Minimum size, minimum cell count and faster design with minimum number of clock cycle is the main feature of the proposed design in comparison with other previous works. Hence, this structure can extensively be as the building block of QCA based circuits.

REFERENCES

[1] International Technology Roadmap for Semiconductors (ITRS), 2013. (Available from: http://www.itrs.net.),accessed date 2013.

[2] Lent CS, Tougaw P D. “A device architecture for computing with quantum dots”. Proceedings of the IEEE 1997; 85:541–557.

[3] B. Sen, et al., "Towards the Design of Hybrid QCA Tiles Targeting High Fault Tolerance," Journal of Computational Electronics, vol. 15, pp. 429-445, Jun. 2016.

[4] Mohsen Hayati and Abbas Rezaei, “Design of novel efficient adder and subtractor for quantum-dot cellular automata” International Journal of Circuit Theory and Applications, 43: 1446–1454. doi: 10.1002/cta.2019.

[5] Hashemi S, Tehrani M, Navi K. “An efficient quantum-dot cellular automata full-adder”. Scientific Research and Essays 2012; 7:177–189.

[6] QCADesigner, 2018. (Available from: https://waluslab.ece.ubc.ca/qcadesigner/qca-designer-downloads/).

[7] Tahoori MB, Momenzadeh M, Huang J, Lombardi F. “Testing of quantum cellular automata”. IEEE Transactions on Nanotechnology 2004; 3(4):432–442.

[8] Dysart TJ, Kogge PM, Lent CS, Liu M. “An analysis of missing cells defects in quantum-dot cellular automata”. IEEE International Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures (NANOARCH ’05) in conjunction with the VLSI Test Symposium, Palm Springs, CA. May 1, 2005.

[9] Fijany A, Toomarian BN. “New design for quantum dots cellular automata to obtain fault tolerant logic gates”. Journal of Nanoparticle Research 2001; 3:27–37.

[10] Latha K, Maharshi MN. “Design of adders using qca”. International Journal of Advances in Engineering & Technology 2013; 6:1750–1759.

[11] B. Sen, M. Dutta, R. Mukherjee, R. K. Nath, A. P. Sinha and B. K. Sikdar, "Towards the design of hybrid QCA tiles targeting high fault tolerance," Journal of Computational Electronics, vol. 15, pp. 429-445, November 2015.

[12] M. Momenzadeh, M. B. Tahoori, J. Huang, and F. Lombardi, "Quantum Cellular Automata: New Defects and Faults for New Devices," in Proceedings of the 18th International Parallel and Distributed Processing Symposium, 2004, pp. 207-214.

[13] G. A. Anduwan, et al., "Fault-tolerance and Thermal Characteristics of Quantum-dot Cellular Automata Devices," Journal of Applied Physics, vol. 107, no. 11, pp. 1134061-10, 2010.

[14] M. A. Amiri, M. Mahdavi, and S. Mirzakuchaki, "QCA Implementation of a MUX-based FPGA CLB," in International Conference On Nanoscience and Nanotechnology, Australia, 2008, pp. 141-144.