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Introduction

1.1 Introduction

While mobile phones enjoy the largest production volume ever of any consumer electronics products, the demands they place on RF/mm-wave transceivers are particularly aggressive, especially on integration with digital processors, low area, low power consumption, while being robust against process-voltage-temperature (PVT) variations. Figure 1.1 (a) illustrates the evolution of data rates for wireless LAN, cellular, and wireline short links over time [1]. Interestingly, there is a constant $\sim 10\times$ increase in bit rate every five years for both wireline and wireless links. Since mobile terminals inherently operate on batteries, their power budget is basically constant. Hence, an ever-decreasing power per bit is required to maintain the system lifetime. As shown in Figure 1.1 (b), the RF front-end circuitry consumes significant power for typical use cases of mobile terminals such as voice call, web browsing and email [2]. Consequently, power efficiency of RF building blocks has become a major issue, especially when designing system-on-chips (SoC) for wireless communications.

On the other hand, in the upcoming years, the wireless Internet-of-Things (IoT) will enable more objects to be sensed and controlled remotely, realizing more integration between the physical and digital worlds. According to communication giant Cisco systems [3] there will be approximately 50 billion Internet-connected objects (things) by 2020, just 2.7 percent of all the things that will be on the planet. However, the system lifetime still tends to be severely limited by its power consumption, available battery technology and efficiency of its energy harvester. Consequently, the key challenge of these wireless sensors is the ability to function at the lowest power possible while being robust to PVT variations. Similarly, the power consumption of RF building blocks should be reduced to satisfy the lifetime demands of IoT systems. Furthermore, RF circuitries such as oscillator and phase lock loop

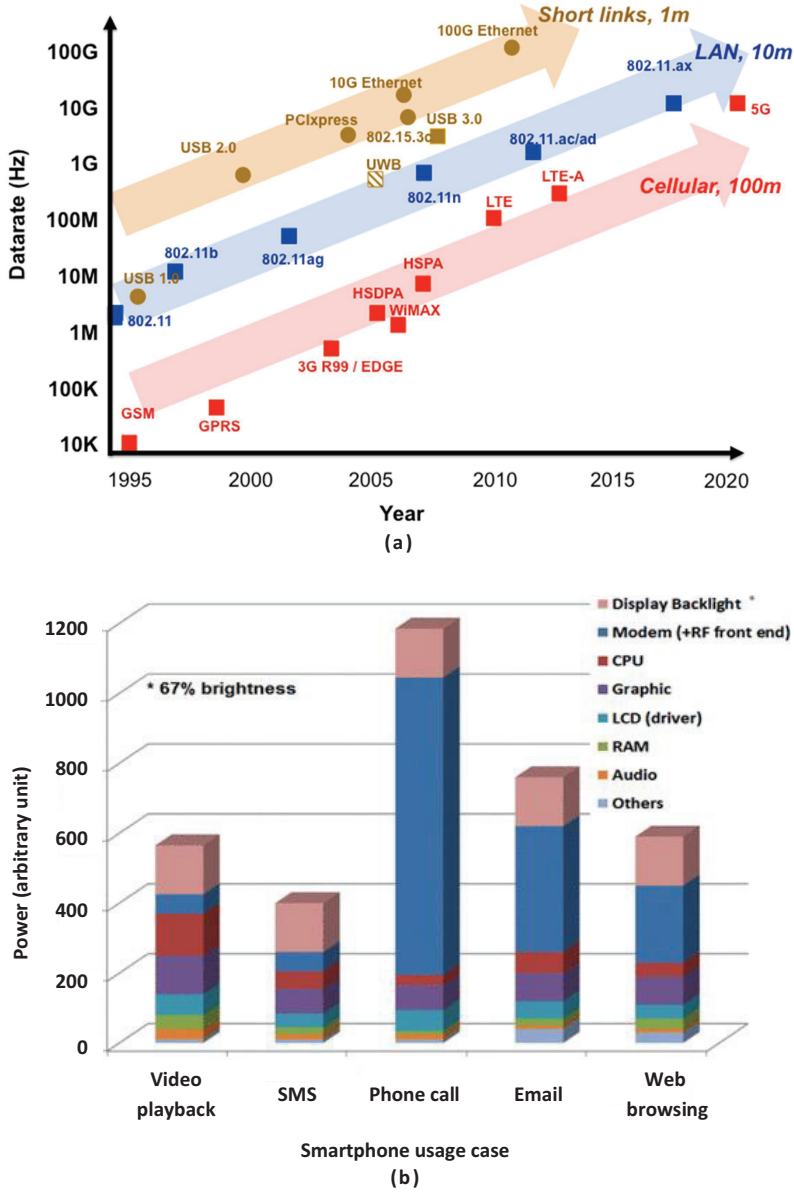

Figure 1.1 (a) Evolution of data rates for wireless LAN, cellular, and wireline short links over time [1]; (b) power usage in a smartphone [2].

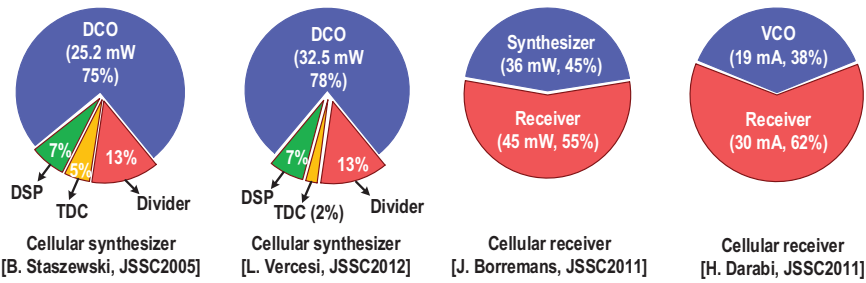

Figure 1.2 Contribution of RF oscillator to the power consumption of cellular frequency synthesizers and receivers.

(PLL) should be able to turn on/off quickly to permit high energy-efficiency during intermittent operation.

The RF oscillator is the second most power hungry block of a wireless radio (after power amplifiers). As shown in Figure 1.2, the RF oscillator consumes a disproportionate amounts of the power of a cellular frequency synthesizer [4, 5] and burns more than 30% of the cellular receiver power [6, 7]. Consequently, any power reduction in an RF oscillator will greatly benefit the overall power efficiency of the cellular transceiver. For IoT applications, the commercial perspective is now focusing on Bluetooth Low Energy (BLE). In the state-of-the-art BLE radios [8–10], the PLL power consumption is merely 3–4× lower than that of power amplifier (PA) at the maximum BLE output power of 1 mW. However, the frequency synthesizer activity is much longer than that of a PA, making the PLL the most energy-hungry block in a BLE transceiver. Consequently, RF oscillators, as one of the BLE transceiver's most power hungry circuitry, must be very power efficient.

On the other hand the RF oscillators' purity limits the transceiver performance. The oscillator's phase noise in a transmit chain results in power leakage into adjacent channels. In the receive chain, the down-conversion of a large interferer with a noisy local oscillator (LO) causes reciprocal mixing. Furthermore, in orthogonal frequency-division multiplexing (OFDM) systems, the phase noise leads to inter-carrier interference and a degradation in the digital communication bit error rate. Table 1.1 summarizes the frequency bands and the phase noise requirement specifications for some communication standards. The trade-offs between oscillator's phase noise and its power consumption introduce a challenge for oscillator designers. To achieve high frequency accuracy, oscillators are incorporated in a PLL (as is shown in Figure 1.3 for both analog and digital PLLs), they can benefit from high pass nature of filtering of their noise by the loop (see Figure 1.4). This reduction

Table 1.1 Communication standards requirements [11]

Standard	Frequency Band (GHZ)	Required Phase Noise (dBc/HZ)
Bluetooth	2.402–2.480	–84 @ 1 MHz –114 @ 2 MHz –129 @ 3 MHz
GSM 900/1800	0.880−0.960 1.710−1.880	−122 @ 0.6 MHz −132 @ 1.6 MHz −139 @ 3 MHz
UMTS	1.920−2.170 1.900−2025	−132 @ 3 MHz −132 @ 10 MHz −144 @ 15 MHz
WiFi	2.412−2.472 5.150−5.350 5.470−5.825	−102 @ 1 MHz −125 @ 25 MHz

of the oscillator's low frequency noise in the synthesizer is highly dependent on the loop bandwidth. The loop bandwidth of the PLL is usually chosen to minimize the noise contribution of the frequency reference and charge pumps. However, if this bandwidth is less than the $1/f^3$ corner of the oscillator then part of the oscillator's low frequency noise remains unfiltered.

Another challenge for the recent RF oscillator designers is the ability to design a wide tuning range oscillator while having low phase noise. The multi-standard applications that are now trending demand such oscillators. The trade-off between the quality factor of the switch capacitor bank that is tuning the LC oscillators and the oscillator's tuning range is the obstacle in wide tuning-range oscillator design. The MOS transistor switch introduces a resistance that defines the switched capacitor bank's quality factor in on-state, consequently a lower resistance and so a larger MOS transistor is required for phase noise consideration. However, in the off-state, the series combination of the capacitor in the tank and the switch's parasitic capacitances defines the equivalent tank capacitance. Consequently a smaller switch is preferred to increase the tuning range. This trade-off makes it impossible to meet both wide tuning range and low phase noise at the same time. For a moderate phase noise, the tuning range of the oscillator can hardly go beyond 50% [13]. Some designers tried to switch inductors or transformers instead of the capacitors in order to increase tuning range, however the equivalent tank's Q-factor and consequently phase noise is degraded due to the switches in the signal path. Furthermore, due to the reduced oscillation voltage that is tolerable by the nano-metric oxide thickness of advanced technologies CMOS process, the low phase noise design is even more challenging.

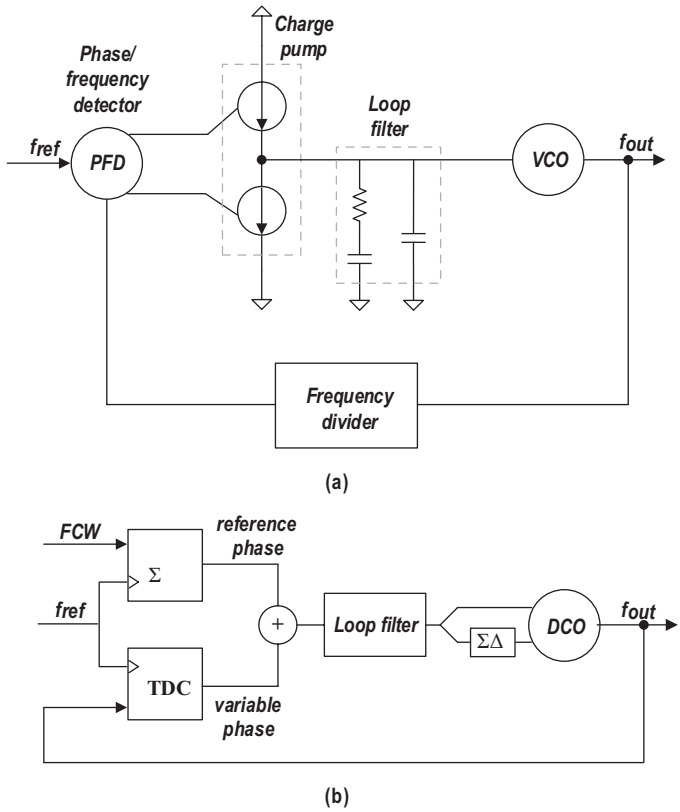

Figure 1.3 (a) Analog and; (b) digital phase locked loops [12].

In this book, the main goal is to to elaborate implementation of innovative RF oscillator structures that demonstrate better PN performance, lower cost, and higher power efficiency than the traditional architectures do.

1.2 Technology Scaling

The size, cost, and power consumption of digital circuits are reduced by technology scaling. However, the design of analog and RF circuits faces many difficulties using more advanced CMOS technologies. Consequently, in the semiconductor industry, there are two divergent trends for choosing a technology node for fabricating analog circuits. One trend is to implement analog circuits in an older technology to exploit a higher voltage headroom. This approach is chiefly used in medical, automotive, and high-efficiency

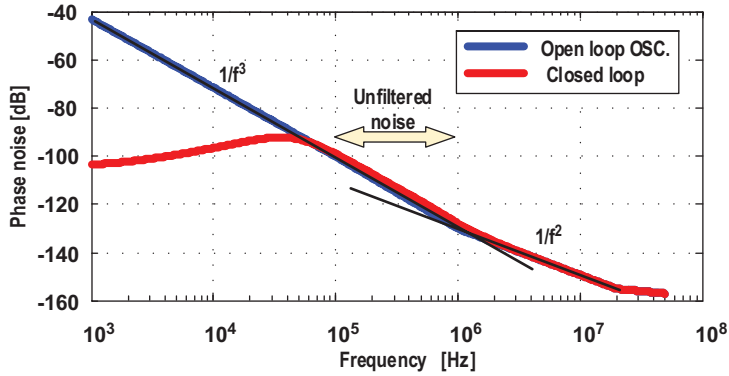

Figure 1.4 Oscillator's open loop and output frequency phase noise.

lighting applications [14]. Another trend is to implement analog and digital circuits together in the most advanced node such as a 16-nm FinFET. The approach is dictated by the market to achieve highest digital performance with lowest fabrication cost.

The vision for both wireless cellular communication and the Internet-of-Things keeps moving towards the second strategy [15]. For example, a few years ego IMEC published the first integrated wireless sensor node in 40-nm CMOS including a microcontroller, digital baseband, power management, and BLE transceiver [8]. Furthermore, Intel and DMCE presented a SAW-less HSPA transceiver with on-chip integrated 3G power amplifiers in 65-nm at ISSCC 2015 to enable real low-cost monolithic system integration [16]. Consequently, it is instructive to investigate the effects of technology scaling on the performance of an RF/mm-wave oscillators.

1.2.1 Supply Voltage

To continue implementing increasingly complex functions while reducing the overall solution costs, scaling of CMOS transistors is inevitable. As circuits become denser, all of the physical dimensions of the transistors must be reduced correspondingly. The SiO_2 oxide-layer thickness reduction is accompanied by migrating to smaller supply voltages (see Figure 1.5). This is to maintain the electric field strength across the oxide in order to prevent the device performance degradation due to the time dependent dielectric breakdown (TDDB) [17]. The supply voltage, V_{DD}, is reduced while RF and analog circuits must maintain their dynamic range, noise performance and output power. For example, the oscillator phase noise performance degrades

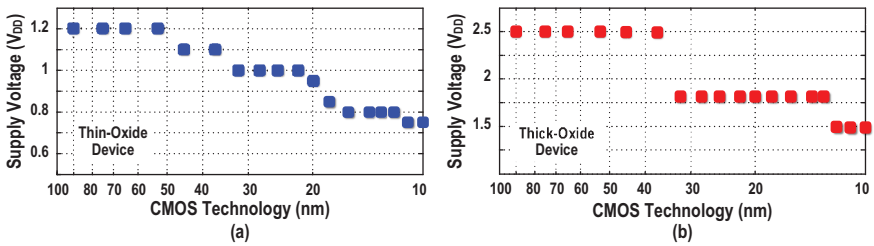

Figure 1.5 Nominal supply voltage versus CMOS technology node for (a) thin-oxide and (b) thick-oxide devices.

by 6 dB/octave with the reduction of their supply voltage [18]. To compensate this phase noise penalty, the equivalent input parallel resistance of an LC tank should be proportionally decreased by reducing the tank's inductance. However, the resistance of the tank's interconnects will start dominating the resonator losses and, consequently, the effective Q-factor and oscillator power efficiency will dramatically drop.

1.2.2 Quality Factor of Passives

Most RF CMOS oscillators employ passive components such as integrated inductors, transformers, and capacitors to realize on-chip LC tanks. Generally, top thick metal layers are used for the realization of inductive components while thinner lower-level metals are exploited in metal-oxide-metal (MoM) capacitors. Note that the 0.18 μm node was the last generation of 8-inch wafer processes with aluminum metallization as almost all modern processes use copper metallization that improves the resistive loss and current handling capability of passive components. Consequently, the quality factor of passives was improved when RF products migrated from 0.18 μm to 0.13 μm technology.

By migrating to more advanced nano-scale CMOS technologies, however, the thickness of lower level metals and interlayer dielectric layers reduce correspondingly as shown in Figure 1.6 (a). As a consequence, the physical dimension of a given capacitance becomes smaller but with a worse quality factor (see Figure 1.6 (b)). Fortunately, the thickness of top thick metal layers almost remains constant with scaling. However, the top-metal is closer to the lossy substrate. Hence, the capacitive parasitic, self-resonant frequency, and quality factor of inductor/transformer slightly degrade with scaling as shown in Figure 1.6 (c).

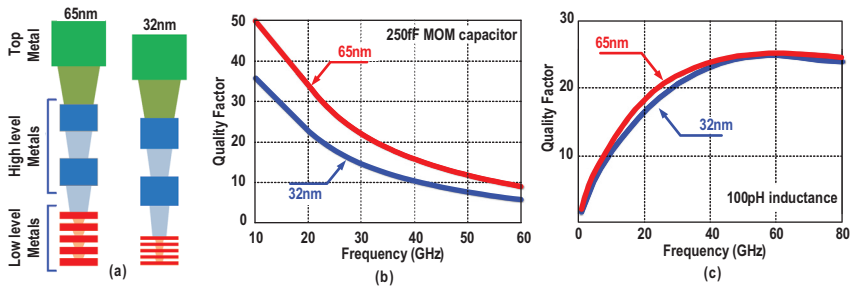

Figure 1.6 (a) Back-end-of-line (BEOL) metallization; quality factor of (b) a 250 fF capacitor, and (c) a 100 pH inductor in 65 nm and 32 nm CMOS technologies [19].

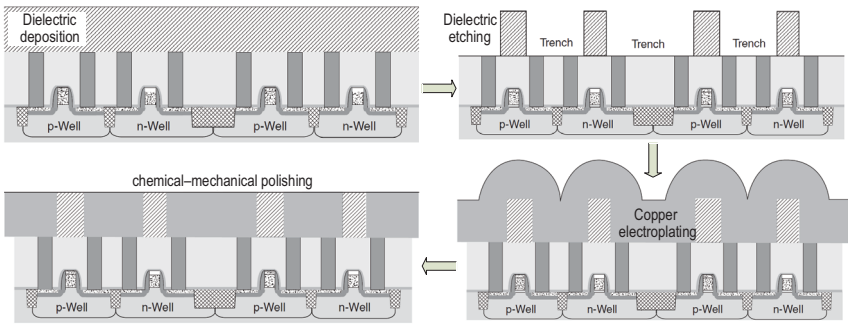

Figure 1.7 Damascene process steps [20].

As mentioned above, in most advanced CMOS technologies, copper is used for interconnections due to its low sheet resistance, high maximum current density, high thermal conductivity and resilience to electromigration failures. However, it is difficult to pattern copper using conventional etching techniques. Consequently, unlike traditional metallization of aluminum, copper metallization needs an additional damascene process as shown in Figure 1.7 [20]. The inter-level dielectric is first deposited in the damascene process. Secondly, the dielectric is etched to define trenches where the metal lines will lie. Thirdly, copper is electroplated to fill the patterned oxide trenches. Finally, the surface is planarized and polished to remove surplus copper outside the desired metal lines using chemical-mechanical polishing (CMP). Unfortunately, CMP suffers from dishing and erosion phenomena. Since copper is much softer than the inter-level dielectric, areas with higher metal density are polished much faster than the others. Consequently, the metal thickness of the sparse areas become thicker than that of the dense

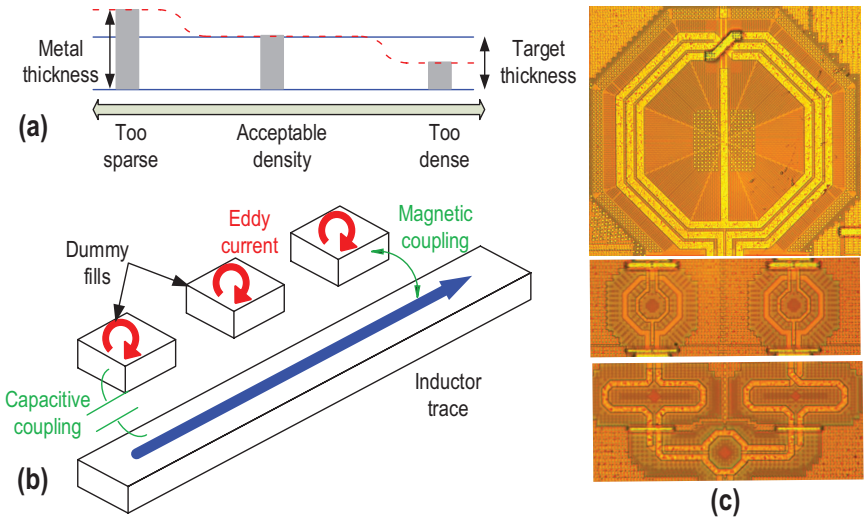

Figure 1.8 (a) Thickness variation by erosion in the CMP stage; (b) electromagnetic coupling between the wire and dummy fills; (c) inductor/transformer with lots of dummy metal fills.

places as shown in Figure 1.8 (a) [22]. To resolve this issue, a minimum metal density must be satisfied for the entire chip. For example, the minimum metal density must be at least 25% in any 100 μm$\times$100 μm square in a 28-nm technology. Hence, inductors and transformers must include dummy metal pieces from the lowest to the highest metal layer (see Figure 1.8 (c)). Metal dummies show negligible effects on the windings self-inductance and the coupling factor. However, as shown in Figure 1.8 (b), eddy currents in dummy fills increase the loss and thus the inductor's/transformer's Q-factor could be degraded by 10% [23].

To conclude this section, the quality factor of passives degrades by migrating to more advanced nano-scale CMOS technologies. It leads to a worse phase noise performance for oscillators.

1.2.3 Noise of Active Devices

Figure 1.9 (a) shows the normalized input-referred 1/f noise, S_{vg}, versus frequency for different technology nodes. Due to oxide scaling enabled by high-k/metal gate technologies, the normalized S_{vg} is monotonically reduced with each successive technology node. For the same transistor area, S_{vg}

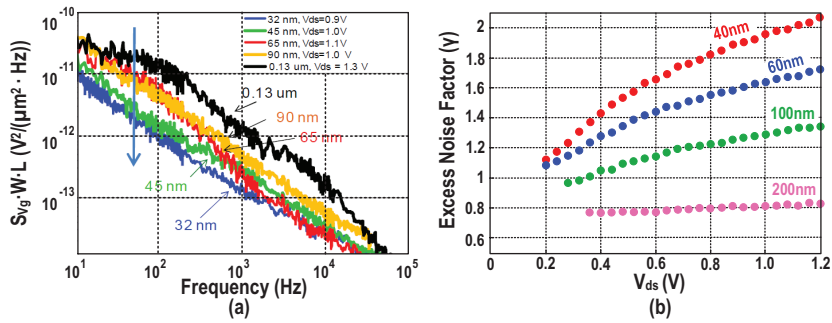

Figure 1.9 (a) Flicker noise scaling trend; (b) measured excess noise (γ) factor versus drain–source voltage at 10 GHz and $V_{gs} = 1.0$ V for different gate lengths of NMOS transistors in 40 nm LP technology [21].

decreases $\sim 10\times$ from the 0.13 μm node to 32 nm node. However, as shown in Figure 1.9 (b), the excess noise factor of CMOS transistors increases by migrating to finer CMOS technologies. Consequently, oscillator's core transistors inject more thermal noise to the tank, degrading its phase noise performance.

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