8

A Study of RF Oscillator Reliability in Nanoscale CMOS

In this chapter, we investigate the nature of oxide breakdown and stress-related degradation mechanisms in MOS transistors. The MOS breakdown time is quantified based on exponential-law and defect-generation models versus the oxide-thickness, gate area, temperature, and voltage stress at a given cumulative failure. As a consequence, a design guide is presented to estimate the time-dependent dielectric breakdown of any analog circuit. Based on reliability analysis, the lifetime of class-F_3 oscillator of Chapter 3 is evaluated for both thin- and thick-oxide options in TSMC 65-nm CMOS process as a case study. The long-term reliability is also investigated for class-F_2 oscillator introduced in Chapter 4.

8.1 Introduction

To keep on implementing increasingly complex functions while reducing the overall solution costs, scaling of CMOS transistors is inevitable. As circuits are growing denser, all of the physical dimensions of the transistors must be reduced correspondingly. The SiO_2 oxide-layer thickness reduction is accompanied by migrating to smaller supply voltages. This is to maintain the electric field strength across the oxide in order to prevent the device performance degradation due to the time-dependent dielectric breakdown (TDDB) [1]. Although digital circuits have fared well, analog designers face additional difficulties with the transistor scaling. The supply voltage V_{DD} is reduced while RF and analog circuits must maintain their dynamic range, noise performance, and output power. For example, the oscillator phase noise performance and power amplifier (PA) output power degrade by 6 dB/octave with reduction of their supply voltage [2, 3]. On the other hand, LC-tank oscillators and PAs usually operate at a voltage swing in excess of the nominal supply voltage. This causes potential reliability issues due to the large electric

field across the gate oxide. Consequently, analog designers must consider the reliability of the circuit while trying to maximize the voltage swing to reach better output power, dynamic range, or noise performance.

In the classical view, the reliability must be qualified at the technology level and guaranteed by the manufacturer. However, this perception is no longer valid. The circuit reliability has become highly circuit-dependent in the advanced CMOS technologies. The designers have to improve the reliability margins by adapting their approach and taking into account the impact of failure at the circuit level. In this chapter, we investigate the nature of oxide breakdown and stress-related degradation mechanisms in MOS transistors. The maximum gate-oxide voltage of a MOS transistor is quantified versus the oxide thickness, gate area, and temperature for different cumulative failure rates and operating times. We exemplify the oxide breakdown reliability calculations in class-F RF oscillators of Chapters 3 and 4.

8.2 Gate-Oxide Breakdown

Gate-oxide breakdown leads to a catastrophic and permanent failure in MOS devices. The breakdown is accompanied by a sudden discontinuous increase in the oxide conductance and the gate current noise. Breakdown is a gradually increasing phenomenon and realized by defects such as electron traps in the oxide structure. The rate of defect generation is almost proportional to the gate current density. As a consequence, the transistors with a smaller channel length are more vulnerable. The gate current is due to Fowler–Nordheim (FN) tunneling for thick-oxide devices at a gate voltage V_g above 3 V, while it is due to a direct quantum-mechanical tunneling (DT) for thin oxides ($t_{ox} \leq$ 3-nm) at voltages below 3 V [4]. These gate currents trigger “impact ionization”, “anode hole injection”, and “trap creation” phenomena to generate defects in the oxide structure. Then, the probable breakdown will occur at a critical trap density by a conduction path via these generated traps. Consequently, the oxide breakdown failure is a time-dependent and statistically distributed phenomenon. It is well known that the oxide breakdown can be described by the Weibull distribution [1]:

$$F\left(T_{BD}\right) = 1 - e^{-\left(\frac{T_{BD}}{\eta}\right)^{\beta}} \tag{8.1}$$

where F is a cumulative failure probability and T_{BD} is a random variable for time-to-breakdown. η is a characteristic time-to-breakdown at 63.2% failure probability and β is a Weibull shape slope.

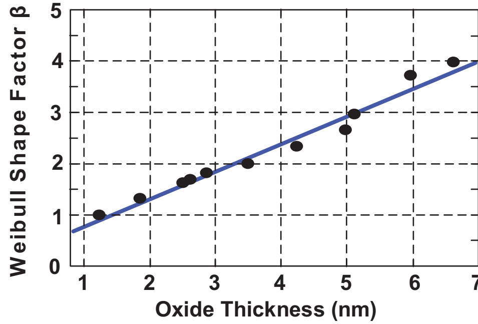

Figure 8.1 Weibull slope versus gate-oxide thickness.

8.2.1 Weibull Slope

Figure 8.1 shows measured Weibull slopes obtained from literature [5] versus oxide thickness ranging from 1.25 to 7 nm at a temperature of 140°C. The solid curve is a linear fit of an analytical cell-based model and expressed by

$$\beta = \frac{t_{int} + t_{ox}}{\alpha_0}, \tag{8.2}$$

where α_0 is the defect size that is found to be 1.83 nm in [5] and t_{int} is the interface thickness, which was reported 0.37 nm in [5]. Equation (8.2) indicates that Weibull slope decreases with the technology scaling. Suppose the η value is the same for both thin- and thick-oxide devices. Although both devices reach the cumulative failure rate of 63% at the same time, the early failure rate of a thin-oxide transistor will be much larger than that of the thick-oxide device due to its lower Weibull slope. Consequently, thin-oxide devices can only tolerate lower electric field strengths for the certain failure rate in a given operating time. It is concluded in [1] that Weibull slope is independent over a wide range of stress voltage, temperature, and polarity.

8.2.2 η Estimation for Different Oxide Thicknesses

Figure 8.2 shows η versus gate voltage for different oxide thicknesses. The data points (open/solid squares, triangles, and circles) are extracted from literature [1, 4, 9] and scaled to 140°C and an area of 10^3 μm^2. The TDDB reliability is usually estimated by means of voltage and temperature acceleration models from results acquired at relatively short measurement times to the required product lifetime of 10 years or more. Such a scaling may span several decades and magnify inaccuracies if the model is not correct or the breakdown mechanism changes along the voltage scaling. Until now, at least

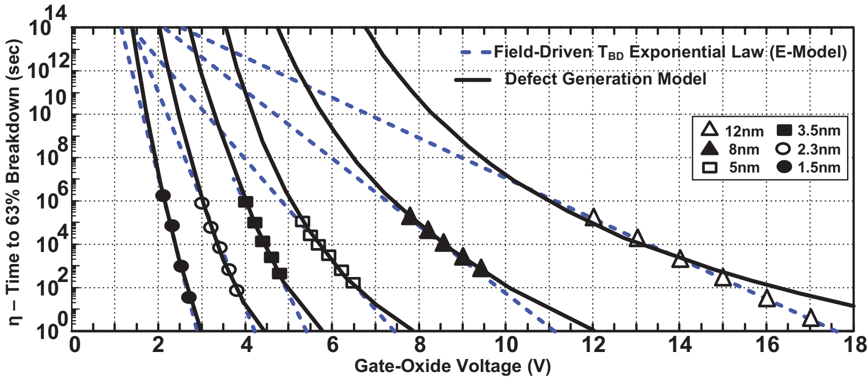

Figure 8.2 Comparison of characteristic time-to-breakdown η versus gate voltage in NMOS inversion for different gate-oxide thicknesses from 1.5 to 12 nm. The solid lines represent the result of defect generation model as described in [7]. The dashed lines are from the least-square fit using the E-model, as described in [9]. The data points (open/solid squares, triangles, and circles) are extracted from literature and scaled to 140°C with an area of $10^3\ \mu m^2$.

five voltage acceleration models have been proposed: E-model, 1/E model, power-law model, 1/V model, and physics-based model. Not surprisingly, it is confusing and practically impossible to decide which model should be used in TDDB calculations.

The field-driven E-model refers to the experimental observation that T_{BD} data can be characterized by $exp(\gamma \cdot E_{ox})$, where the electric field E_{ox} is considered as a variable in TDDB process [9]. The η variations based on E-model curve fitting are illustrated by dashed lines in Figure 8.2 for different oxide thicknesses. The model can be safely ruled out for both thin and thick oxide at $E_{ox} \geq 7$ MV/cm. However, an extrapolation to lower fields would result in a cross-over between the dashed lines meaning thick-oxide devices are less reliable than thin-oxide ones at voltages below 1.5 V, which is contradictory to the fundamental physics. Consequently, this model is not accurate at $E_{ox} \leq 7$ MV/cm. Nevertheless, it is possible to use E-model as a conservative projection. Hence, E-model estimation has been added in Figure 8.2 as the worst case in T_{BD} prediction [7].

The anode injection model (1/E model) characterizes T_{BD} based on the FN tunneling current. However, the direct tunneling is a dominant phenomenon at $V_g \leq 4$ V. Hence, 1/E model is not applicable and leads to optimistic results at lower voltages [8].

A more realistic projection is the physics-based breakdown model, which considers both tunneling current and defect generation phenomena.

This model is consistent with many measurement results up to the 8-nm oxide thickness. The discrepancy at thicker oxides originates in "band-to-band ionization", which plays an important role in very thick oxides stressed at relatively high voltages [7]. The η extrapolation based on "defect-generation" model is also added by solid lines in Figure 8.2 for different oxide thicknesses.

8.2.3 Area and Temperature Dependence of T_{BD}

The failure of an entire IC chip is defined by the first failure of a single device. From elementary statistics, if the failure probability of a unit is F_{A1}, then the failure probability of a circuit comprising N independent units is given by

$$F_{A2} = 1 - (1 - F_{A1})^N . \tag{8.3}$$

By substituting (8.1) into (8.3) and carrying out lengthy algebra, the area scaling equation of η is obtained by

$$\eta_2 = \eta_1 \left(\frac{A_1}{A_2}\right)^{\frac{1}{\beta}} , \tag{8.4}$$

where A_1 and A_2 correspond to two different areas of the oxide. This expression shows that the characteristic breakdown time, η, increases with reducing the oxide area. The area scaling is a strong function of the Weibull slope and, consequently, thinner oxides are more sensitive. For example, in 10^{-4} to 10 mm^2 area scaling, T_{BD} lifetime drops with 3–4 orders of magnitude for a 4-nm oxide. However, the T_{BD} reduction would be just a factor of 2 for an 11-nm oxide.

The following equation expresses the dependency of η on the oxide junction temperature [6]. As expected, higher temperatures accelerate the TDDB process.

$$\frac{\eta_2}{\eta_1} = e^{\frac{E_a}{K_B}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)} , \tag{8.5}$$

where K_B is the Boltzmann's constant and E_a is the thermal activation energy that is about 1 eV and changes by a small amount with the gate voltage [6].

8.2.4 Principle of Extrapolation to a Specified Condition

Figure 8.2 shows the extrapolated η for physics-based and E models for an area 10^3 μm^2 at 140°C. The main question arises: How can one predict

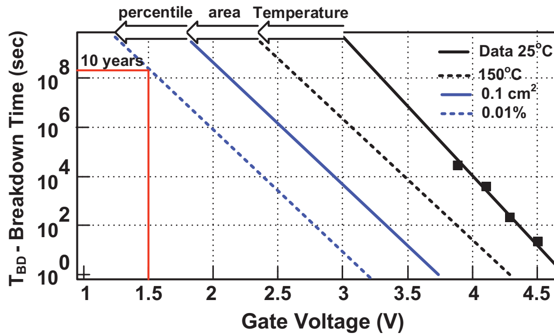

Figure 8.3 Extrapolation steps to the specified condition.

TDDB lifetime of a circuit for a given voltage and cumulative failure values based on this figure? The principle of T_{BD} extrapolation to a specified condition is illustrated in Figure 8.3. As a first step, one of the curves in Figure 8.2 is chosen based on the technology oxide thickness. This curve will shift through (8.5) if the operating temperature deviates from the reference value 140°C. Then, the area scaling is applied to the graph using (8.4). The curve is scaled once more to the desired cumulative failure by (8.1). Finally, the corresponding T_{BD} can be calculated from the obtained curve (blue dashed-line in Figure 8.3) for any gate voltages.

8.3 Hot Carrier Degradation

Hot carriers (HC) are holes or electrons that are accelerated to high energies by an electric field caused by a large drain–source voltage. Certain percentage of the hot carriers collide with the lattice and create electron–hole pairs. Furthermore, if the hot charge carriers have a kinetic energy larger than the silicon-oxide barrier height, some of them will dominate the barrier and flow toward the insulator.

Unlike the gate-oxide breakdown, this phenomenon is not inherently catastrophic. Instead, it can cause a gradual performance degradation during the operating lifetime. These traps can shift the threshold voltage and reduce the conducting carrier mobility. Consequently, the drain current, channel resistance, and transconductance gain of MOS transistor decrease and degrade performance of RF circuits, such as oscillators. First, one needs to choose larger gm-devices to compensate the oscillator loop gain reduction due to HC. It means the active device injects more noise into the tank, resulting in an increase of the oscillator's effective noise factor. Furthermore,

the circuit phase noise performance gradually degrades due to reduction of drain current and thus the oscillation voltage swing. Hence, an additional mechanism should sense the oscillation amplitude in order to increase the drain current of active devices by adjusting their bias voltage. Second, a combination of a large parasitic capacitance of the tail current transistor and a smaller channel resistance of the gm-device could provide a discharge path between the tank and ground. It would drop the equivalent quality factor of the tank resulting in phase noise degradation. Third, hot carrier stress also increases the $1/f$ noise of the MOS transistor, which is translated to a larger $1/f^3$ oscillator phase noise corner.

However, the hot carrier degradation mainly occurs when the drain current and drain–source voltage are substantial at the same time [3]. Hence, the hot carrier degradation would be negligible if the channel current was low when the drain–source voltage was high and vice versa. This condition naturally occurs in oscillators and switching power amplifiers. Consequently, the RF oscillators are not inherently vulnerable to the hot carrier degradation.

8.4 Negative Bias Temperature Instability

The negative bias temperature instability (NBTI) occurs when a negative gate–source voltage V_{gs} is applied causing an increase in the absolute threshold voltage, a degradation of the mobility, drain current, and transconductance. PMOS devices are more vulnerable to NBTI. Although NMOS devices can be damaged in an NBTI stress, the damage occurs at negative V_{gs} where NMOS devices are not active. Consequently, NMOS devices are thus suggested for long operating time applications such as infrastructure basestations and satellite communications.

8.5 Reliability of Class-F_3 Oscillators

8.5.1 Class-F_3 Oscillators

Figure 8.4(a) shows a schematic of the class-F_3 oscillator in Chapter 3, which was realized in TSMC 65-nm CMOS technology. It exhibits a pseudo-square-wave across the tank to desensitize the oscillator phase noise to the circuit noise. Figure 8.4(b) illustrates the oscillation waveforms. As can be seen, gate–drain voltage increases to 3.2 V at 1.2-V supply voltage due to the passive voltage gain of the transformer. $M_{1/2}$ dimensions should be (48-$\mu m/0.28$-μm) and (12-μm/65-nm) for thick (5 nm) and thin (2.3 nm)

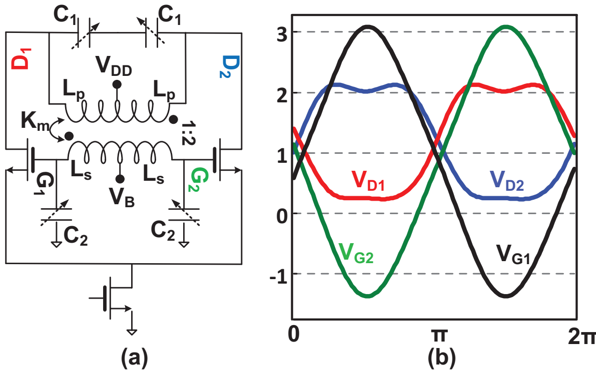

Figure 8.4 Class-F oscillator: (a) schematic; (b) waveforms.

oxide options, respectively, to guarantee safe oscillator start-up in all process corners. Let us investigate the oscillator's lifetime at 0.01% cumulative failure rate and 140°C for both transistors. From Figure 8.5, the η values are obtained as

$$\eta_{thin}\left(10^3\mu m^2\right) = 10^5 s, \quad \eta_{thick}\left(10^3\mu m^2\right) = 10^{10} s. \tag{8.6}$$

The conservative E-model is used for the T_{BD} calculations. Weibull slope should be determined in order to extrapolate η values to the desired area. Based on (8.2),

$$\beta_{thin} = 1.5, \quad \beta_{thick} = 3. \tag{8.7}$$

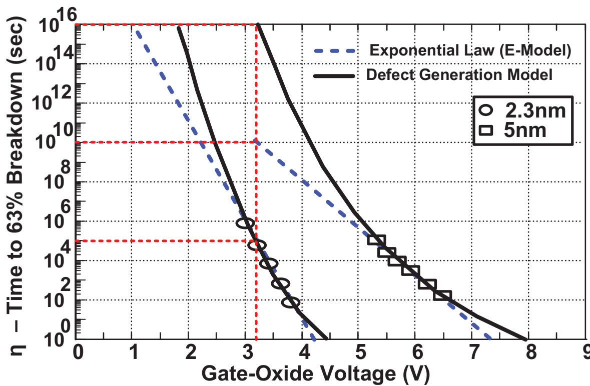

Figure 8.5 Class-F$_3$ oscillator lifetime estimation due to TDDB for thin- and thick-oxide transistors.

The next step is to apply the area scaling factor to η by (8.4).

$$\eta_{thin}\left(1.6\mu m^2\right) = 7\cdot 10^6\text{s},\ \ \eta_{thick}\left(27\mu\text{m}^2\right) = 3\cdot 10^{10}\text{s}. \tag{8.8}$$

Finally, the lifetime can be estimated by substituting the calculated parameters in (8.4):

$$T_{BD}\left(thin\right) = 4\ hours,\ \ T_{BD}\left(thick\right) = 40\ years \tag{8.9}$$

The oscillator lifetime drops dramatically by 4 orders of magnitude just by replacing thick-oxide gm-devices with thin-oxide ones. Consequently, a thick-oxide device must be used in the class-F_3 oscillator to satisfy the required T_{BD} and failure rate but at a cost of more parasitic capacitance and lower tuning range.

8.5.2 Class-F_2 Oscillators

The HCI degradation would occur when the drain current, I_{DS}, and drain–source voltage, V_{DS}, are large at the same time. Thanks to the transformer's voltage gain, in class-F_2 oscillator, V_{DD} is low enough such that V_{DS} of its gm-devices can be much less than the standard voltage of thick-oxide transistors (2.5 V) when they operate in on-state (see Figure 4.11). Consequently, this oscillator is not inherently vulnerable to HCI. However, the large oscillation swing applies a strong electric field across the gate oxide of gm-devices (V_{DG}, V_{GS}), which can potentially reduce the long-term reliability of the oscillator due to TDDB.

The oxide breakdown stems from defects, such as electron traps, in the oxide structure. The rate of defect generation is almost proportional to the gate-oxide electric field and its leakage current density. We can re-write Equation (8.1) as

$$\eta = T_{BD}\left(-ln\left(1-F\right)\right)^{-1/\beta}. \tag{8.10}$$

It is shown in [1] that η for a given circuit with arbitrary characteristics (A_{ox}, V_{ox}, and T_{ox}) can be extrapolated from the reference data (x_{ref}) by

$$\eta = \eta_{ref}\left(\frac{V_{ox}}{V_{ref}}\right)^{-n} e^{\frac{E_a}{K}\left(\frac{1}{T_{ox}}-\frac{1}{T_{ref}}\right)}\left(\frac{A_{ox}}{A_{ref}}\right)^{-1/\beta}. \tag{8.11}$$

where n is voltage acceleration factor.

We can apply the above procedure to our class-F_2 oscillator to determine its T_{BD}. Figure 8.6(a) shows the measured F versus T_{BD} for 14 samples

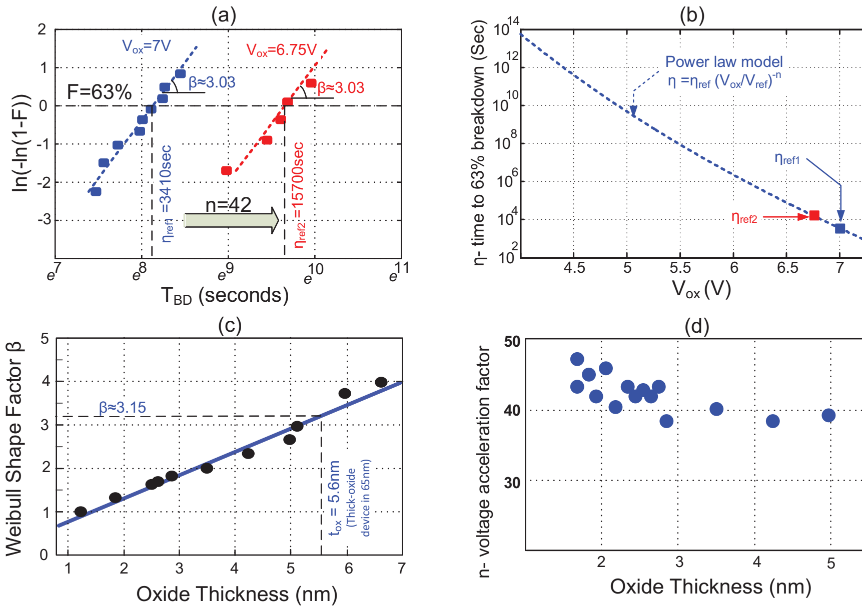

Figure 8.6 (a) Measured cumulative failure rate F versus breakdown time T_{BD} for 14 samples of a thick-oxide transistor (176 μm/0.28 μm) at room temperature, (b) the projected η value versus different gate-oxide stress voltage based on the measured η_{ref}, (c) Weibull slope versus gate-oxide thickness extracted from measurement results in [1], and (d) voltage acceleration versus gate-oxide thickness extracted from measurement results in [10].

of the thick-oxide transistor (176 μm/0.28 μm) at room temperature when a large voltage (6.75 and 7 V) is applied across the gate. The data points are easily mapped to a Weibull distribution curve as indicated by the dashed line. The cross-over of these curves at $F = 63.2\%$ specifies the reference η values (η_{ref}). The voltage acceleration ratio n is calculated by applying η_{ref} values and their related V_{ox} in (8.11). Furthermore, the slope of the curves determines β. Consequently, the estimated n and β values are, respectively, 42 and 3 for the thick-oxide devices ($t_{ox} = 5.6$ nm) in 65-nm CMOS, which are close to extracted measured numbers from literature, as shown in Figure 8.6(c,d) [1, 10]. The E_a is ∼0.55 eV and independent from the oxide thickness and temperature [11]. Consequently, the given oscillator η can be estimated by substituting the measured reference and technology parameters and circuit characteristics (A_{ox}, V_{ox}, and T_{ox}) in (8.11). Finally, T_{BD} is calculated by substituting the estimated η and the desired F in (8.10).

The lifetime estimation of our circuit as a function of V_{ox} is plotted in Figure 8.7 for various F, T_{ox}, and A_{ox}. The plots indicate that the maximum voltage across the oxide for $M_{1,2}$ transistors should be <4.4 V to ensure $<0.01\%$ failure during 10 years at 125°C. The max V_{ox} could be increased if higher failure rate or lower max operating temperature are accepted. The maximum dc voltage is thus established across the gate oxide. However, the actual nature of stress in RF oscillators is not dc but an ac voltage $V_{ox}(\omega_0 t)$. Consequently, it is instructive to compare the static max V_{ox} with the actual operation when η changes over the period of the resonant frequency. Hence, the "effective" η is calculated as

$$\frac{1}{\eta_{\text{eff}}} = \frac{1}{2\pi} \int_0^{2\pi} \frac{1}{\eta \left(V_{ox}\left(\omega_0 t\right)\right)} \, d\left(\omega_0 t\right), \tag{8.12}$$

where $\eta(V_{ox}(\omega_0 t))$ is given by (8.11) and can be expediently simplified to $\eta = B \cdot (V_{ox}(\omega_0 t))^{-n}$.

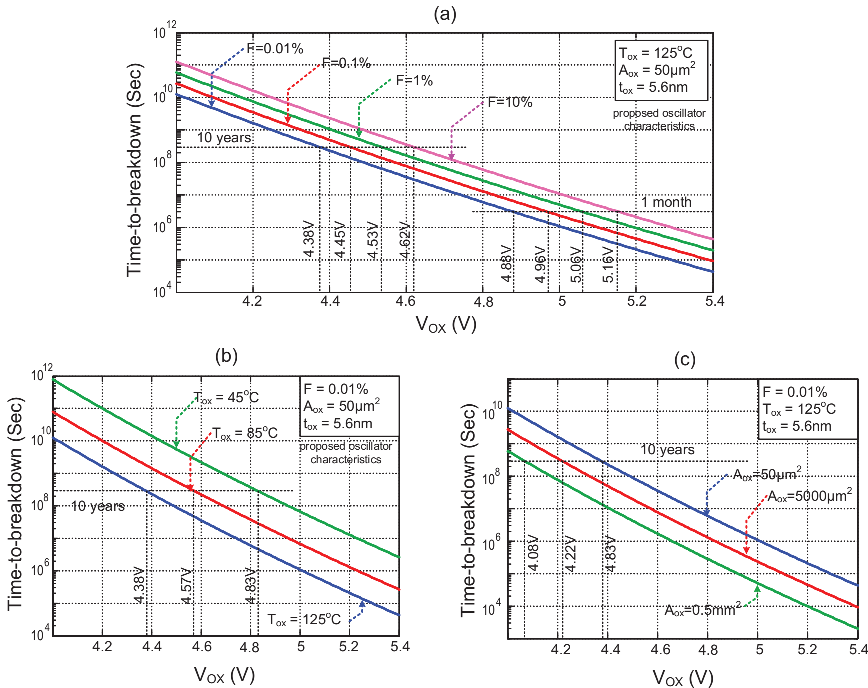

Figure 8.7 Estimated time-to-breakdown (based on the measured parameters of Figure 8.6(a)) of thick-oxide transistors in 65-nm CMOS versus maximum gate-oxide stress voltage for different (a) cumulative failure rates, (b) temperatures, and (c) gate-oxide areas.

Starting with the application's desired operating time (i.e., T_{BD}) at a given failure rate (F) in a given technology (i.e., β), the parameter η_{eff} is first established as per (8.10) and is identical for dc and ac operations. For a dc operation, $\eta = B \cdot (V_{dc})^{-n}$ and (8.12) results in

$$V_{dc} = \left(\frac{B}{\eta_{\text{eff}}} \right)^{1/n}. \tag{8.13}$$

However, for an ac operation,

$$\frac{1}{\eta_{\text{eff}}} = \frac{1}{2\pi} \int_0^{2\pi} \frac{1}{B \left(0.5 V_{ac,max} \left(1 + sin\left(\omega_0 t\right)\right)\right)^{-n}} \, d\left(\omega_0 t\right). \tag{8.14}$$

Solving this integral for the voltage acceleration factor n of 42 for the 65-nm CMOS thick-oxide devices,

$$V_{ac,max} = \left(\frac{11.5 \cdot B}{\eta_{\text{eff}}} \right)^{1/n}. \tag{8.15}$$

Consequently, the ac to dc maximum tolerable stress voltage ratio ($V_{ac,max}/V_{dc}$) will be $(11.5)^{1/n} \approx 1.06$. We strongly emphasize that there are no significant differences in max V_{ox} at ac-peak and dc conditions due to the sharp slope of $T_{BD} - V_{ox}$ curves in Figure 8.7. As shown by integrating the voltage-dependent $\eta(V_{ox})$ over the full oscillation cycle, the peak magnitude of the V_{ox} sine wave can be just 6% higher than what is determined for a fixed dc V_{ox}. Consequently, the slightly lower pessimistic value of V_{ox} in the dc condition could be used as an extra margin.

8.6 Conclusion

Time-dependent dielectric breakdown (TDDB), hot carrier degradation (HCI), and negative bias temperature instability (NBTI) mechanisms were investigated for a MOS transistor. The exponential-law and defect-generation models quantified the MOS breakdown lifetime versus the oxide-thickness, gate area, temperature, gate voltage, and cumulative failure rate. A design guide is presented to estimate TDDB of any analog circuit. Based on reliability analysis, a huge 4-decade lifetime difference exists between thin (2.3-nm) and thick (5-nm) oxide devices in the class-F_3 oscillator. The reliability process is highly circuit-dependent in the advanced CMOS technologies (oxide thickness $\leq$ 3 nm) and analog/RF engineers have to consider the reliability issues in the design cycle.

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