6

FM-UWB Transceiver

6.1 Introduction

The previous chapter dealt in details with the implementation of the quadrature approximate zero-IF receiver. The next step is to integrate a full FM-UWB transceiver. Aside from the quadrature AZ-IF receiver, that provides the multi-user communication capability, the single-ended receiver is added, and can be used to reduce the power consumption of the transceiver when lower performance is acceptable. Furthermore, the integrated transceiver includes a baseband that performs the sub-carrier FSK demodulation and symbol clock recovery, and provides fully digital outputs that can be interfaced by an FPGA or a microcontroller. Although there are no major architectural innovation on the transmitter side, the clever use of circuit techniques provides means for some improvements compared to the state of the art in terms of power consumption and efficiency. The emphasis is on the fully integrated output matching network, that allows to use the same RF pad for both reception and transmission, eliminating the need for an external switch or any other passive components.

First, the top level architecture of the transceiver is described. Then, in the following section, the details of transmitter circuit implementation are given, followed by the circuit implementation of the two receivers in Section 5.3. The results of transceiver characterization are presented in Section 5.4, demonstrating the capabilities of the proposed approach with emphasis on robustness and low power consumption. Finally, the chapter is concluded with the summary of performance and comparison with the state of the art.

6.2 Transceiver Architecture

The implemented FM-UWB transceiver consists of two receivers and a transmitter (Figure 6.1). Aside from low power consumption, the emphasis of this

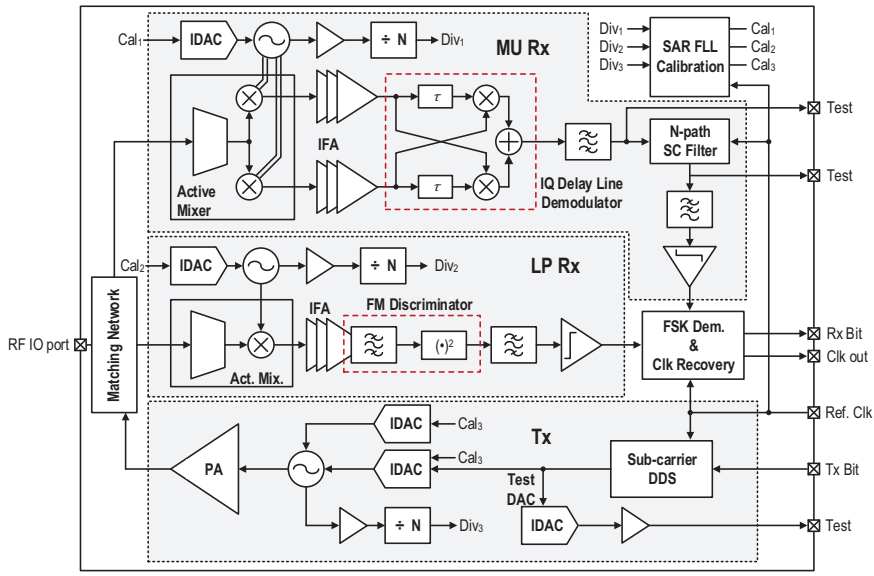


Figure 6.1 Top-level block diagram of implemented transceiver.

work is also on high level of integration and miniaturization, robustness to narrowband interferers and tolerance to reference frequency offset. A single RF pad is used as both receiver input and transmitter output, eliminating the need for an off-chip switch that was needed in all the previous implementations found in the literature. In addition, the matching network is fully integrated and no passive components need to be added externally.

Large signal bandwidth of the FM-UWB signal means that the transceiver inherently possesses some robustness against the RF carrier frequency offsets. In the baseband section of the receiver, a relatively small offset (e.g. less than 0.5%) between the transmit and the receive symbol clock can be compensated using a simple clock recovery scheme. As a result, there is no need for a precise frequency reference in the system and no need for a crystal oscillator. Instead, an RC reference oscillator can be integrated on-chip and calibrated before use, allowing to completely remove all the external components.

Just like in the previous section, the LO signal is generated using ring oscillators. Owing to the loose phase noise constraints and the large signal bandwidth, such an approach is acceptable and is exploited to reduce the receiver power consumption. Normally, ring oscillators operate in a loop that stabilizes the oscillation frequency (PLL), however here they are used

in a free-running mode so as to reduce the significant power overhead that would otherwise be present due to continuous operation of frequency dividers. Instead, the oscillators are periodically calibrated using a successive approximation register (SAR) FLL, assuring that the frequency offset remains within the required limits.

The transmitter architecture is similar to other implementations found in the literature. The sub-carrier signal is synthesized digitally, allowing easier control and switching of sub-carrier frequencies, as well as better precision compared to an analog solution with a capacitor bank. The sub-carrier signal is used to drive a current DAC that controls the DCO frequency, that finally produces the desired FM-UWB signal. The resulting signal is then amplified by the preamplifier (PPA) and the power amplifier (PA) before transmission.

The two implemented receivers are intended for two modes of operation. The multi-user (MU) receiver consumes more power and is capable of distinguishing multiple FM-UWB signals and providing SC-FDMA. Its purpose is to provide multiple channels and speed up communication when network traffic is high. It is based on the receiver described in the previous section with the addition of the channel filtering and baseband processing. The low power (LP) receiver provides a low power, low performance mode, that can be used when the network traffic is low and a single channel is sufficient. Instead of quadrature demodulation, it only uses a single branch, allowing to simplify the receiver architecture and save power. However, due to the non-linearity of the frequency-to-amplitude conversion characteristic of the demodulator, it cannot distinguish multiple channels allowing only a single FM-UWB user.

6.3 Transmitter Implementation

A more detailed block diagram of the transmitter is given in Figure 6.2. The DCO is in fact driven by two DACs. The first one, referred to as the static DAC, only determines the highest frequency in the FM-UWB signal spectrum f_H. Its output remains constant during transmission. The second DAC, or the dynamic DAC, is driven by the digital sub-carrier signal and controls instantaneous frequency of the DCO, and hence all the modulation characteristics. Two DACs are calibrated prior to transmission using an on-chip SAR FLL. In the first step, the static DAC is calibrated to set f_H. In the second step, the dynamic DAC is calibrated to set the FM-UWB signal bandwidth. The third DAC is added for testing purposes. It is an exact copy of the dynamic DAC that provides the sub-carrier signal at its output, allowing to verify the correct operation of the SC-DDS and to measure the sub-carrier frequency.

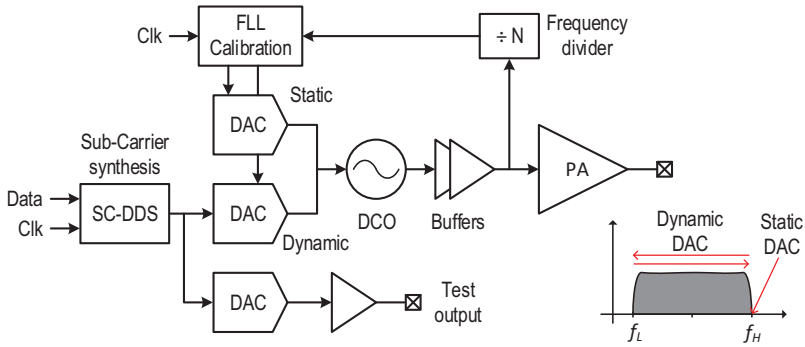


Figure 6.2 Block diagram of the implemented transmitter.

The DCO is separated from the PA and frequency dividers by buffers. These buffers prevent frequency pulling that might be caused by an outside signal, or by the change in capacitance value in the on and off state of the frequency divider. The frequency divider is implemented in the same way as in the receiver described in the previous chapter. It is a chain of ten divide-by-2 circuits from [1] that provide the signal for calibration. The divider buffer, that is needed to amplify the DCO signal and provide the rail-to-rail swing at its output, is adjusted here for a single-ended input.

6.3.1 Sub-Carrier Synthesis

The sub-carrier synthesizer is a fully digital block that provides a 6 bit value at its output. This implementation is following the principles described in [2]. The sub-carrier signal is generated in two steps. First, an accumulator generates a saw-tooth waveform, and then in the second step this saw-tooth waveform is folded to produce a triangular waveform. The frequency of the sub-carrier is controlled by controlling the slope of the saw-tooth waveform, or equivalently the increment value of the accumulator (SC1 and SC2 in Figure 6.3). The sub-carrier frequency is given by

$$f_{sc} = f_{clk}\frac{M}{2^N}, \tag{6.1}$$

where f_{clk} is the input clock frequency, N is the number of bits of the accumulator, and M is the increment. Although only 6 bits are used to control the DAC, 16 bits are used for the accumulator to provide the needed frequency resolution. Nominal clock frequency is 40 MHz, which results in frequency resolution of approximately 600 Hz, which is more than enough

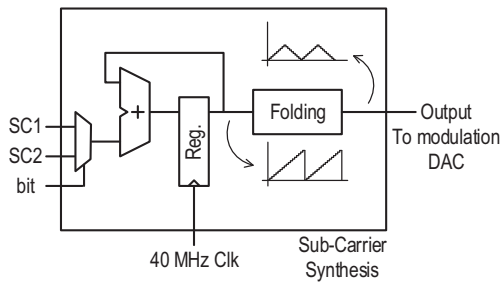


Figure 6.3 Digital sub-carrier synthesizer.

to generate a 100 kb/s FSK signal with a modulation index of 1. No pulse shaping or filtering is used in this implementation. Compared to fully analog implementations, such as those described in [3, 4], DDS approach requires slightly more power. However, since the SC synthesizer consumption is typically small compared to other blocks in the transmitter, this overhead is negligible, and DDS provides better frequency precision (relative to the reference clock) and easier control, both highly desirable especially in a multi-user scenario.

6.3.2 DCO Digital to Analog Converters

Two current mode digital to analog converters are used to drive the current starved ring oscillator, as explained previously. The static DAC is used to set the high frequency of the FM-UWB signal f_H and the dynamic DAC is used to generate the FM-UWB modulation.

The static DAC is shown in Figure 6.4. Digital control word can be either written manually, using the SPI bus, or a calibration loop can be used to set the register value. Once set, the control word remains constant throughout the transmission. Therefore, there are no specific constraints regarding speed or glitches, and a relatively simple solution can be used. Six bits ($b_0 - b_5$) control the binary weighted current mirror that provides the bias current of the ring oscillator. Although linearity is not paramount for the static DAC, a relatively good characteristic is obtained (as shown in Figure 6.9). The only requirement of this DAC is monotonicity of the characteristic, that is needed to assure the proper functionality of the SAR FLL calibration scheme. Considering that only 6 bits are used, no special matching techniques are necessary to achieve the desired precision.

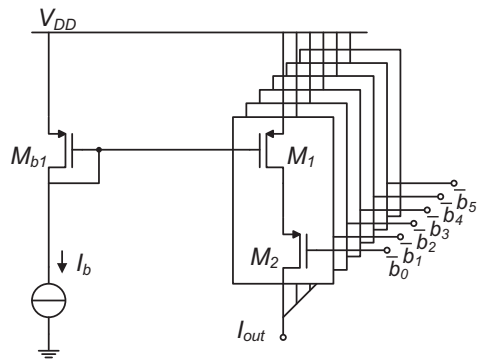


Figure 6.4 Static DCO current DAC.

The dynamic DAC is shown in Figure 6.5. This DAC is actually sinking current from the static DAC. As the value of the digital control word increases, so does the current, effectively reducing the bias current of the oscillator and consequently its frequency. This approach keeps current of the static source constant and provides the good linearity needed for FM-UWB signal generation. As opposed to the static DAC, cascode current mirror is used here, in order to provide better precision of the output current. The dynamic DAC is controlled by the digital sub-carrier signal, which means that it must operate at the clock frequency of 40 MHz, even though the sub-carrier frequency is below 2.5 MHz. For this reason, the current steering approach is used. In this way, the bottom reference transistors M_3 and M_4 never switch off, and there is no additional delay coming from the time required for transistors to turn on (time it takes to charge gate capacitance through the bias transistors M_{b1} and M_{b2}). As a consequence, this technique produces smaller glitches at the output. A capacitor is placed at the output of the two DACs to filter the DCO current and avoid sharp pulses in DCO supply current.

Bandwidth of the FM-UWB signal is controlled using the reference current I_b. The sub-carrier DDS signal always produces a full scale DAC output (all 6 bits are used), and the reference current determines the maximum value of the current, and subsequently the lower frequency f_L. The reference current is generated using yet another current DAC (again static during transmission), with a 5 bit resolution. To calibrate the reference current, bits b_0 to b_5 are all set to '1', resulting in the maximum output current, and then the SAR FLL sets the control bits of the reference current DAC to provide the desired lower frequency f_L. In this way, FM-UWB bandwidth is entirely decoupled from the sub-carrier generation.

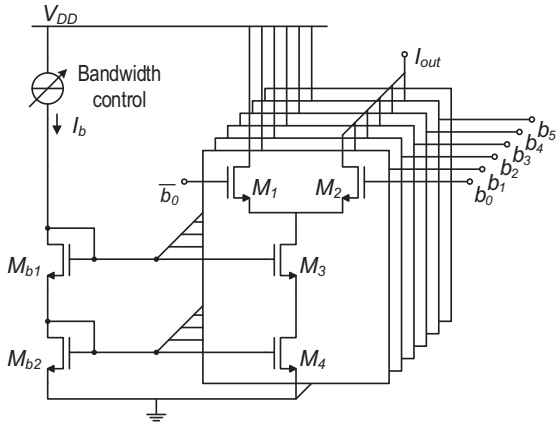


Figure 6.5 Dynamic DCO current steering DAC.

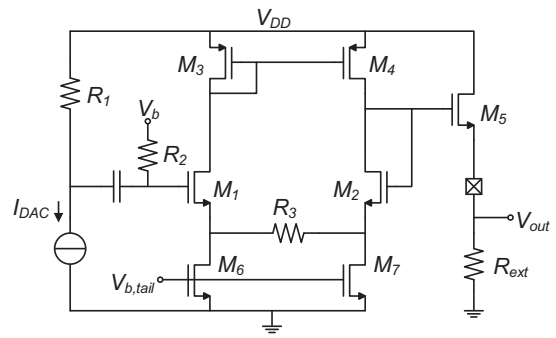


Figure 6.6 Dynamic DAC test output buffer.

As explained above, an exact replica of the dynamic DAC is added for testing. This DAC is driven from the same SC DDS circuit, and will add additional capacitive load to its output. However, since the consumption of the SC DDS remains negligible compared to the DCO and the PA, presence of the testing circuits will not have a significant impact on the overall power consumption. The test DAC drives a buffer that provides analog sub-carrier signal at its output. Resistor R_1 converts the DAC output current into the input voltage of the buffer. This buffer is shown in Figure 6.6. Its main purpose is to verify the sub-carrier frequency. It consists of a resistively degenerated differential pair and a source follower that provides a low impedance output capable of driving a 10 pF capacitive load. Bias current and bandwidth of the source follower are set by the external resistor R_{ext}.

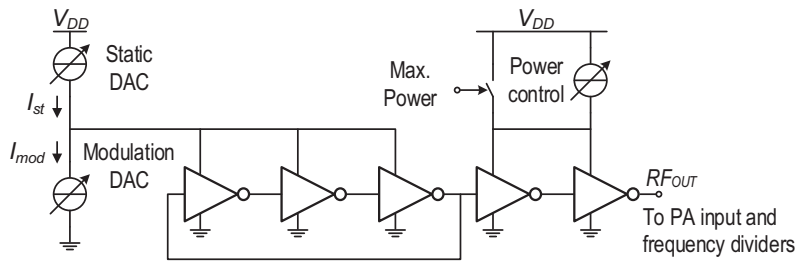


Figure 6.7 Transmitter DCO with buffers.

6.3.3 DCO

The implemented transmitter DCO is shown in Figure 6.7. Since only a single-ended output is needed, the simplest topology, that consequently consumes the lowest amount of power for a given frequency of oscillation, is used. The three inverters of the ring oscillator are scaled progressively, with increasing transistor width from left to right (for both NMOS and PMOS). This was done to increase the driving capability of the inverter driving the buffer, without increasing the overall power consumption. A ring oscillator that is not fully symmetric, i.e. with different stages, generally exhibits higher phase noise [5]. However, in this case symmetry is already broken by the presence of the buffer, and phase noise is not a limiting factor due to the large signal bandwidth, allowing to concentrate on power reduction.

Buffers are placed between the DCO on one side and preamplifier and frequency divider driver on the other. Since the input capacitance of the driver changes in on and off state, buffer is needed to avoid frequency shift after calibration. In addition, it provides isolation in order to avoid frequency pulling if a strong external signal is present. The buffer inverters are current starved, allowing to control the output amplitude by controlling the supply current. There is also a possibility to bypass the current source and connect the buffers directly to the supply voltage, providing the maximum amplitude. Driver of the frequency divider (shown in Figure 6.8) is needed to amplify the DCO output and provide a rail-to-rail signal. It is designed to provide a rail-to-rail signal for a minimum input amplitude of 10 mV, at 5.5 GHz. It consists of 5 inverter stages, two of which are self biased using a large resistor. Since the driver will be on only when calibration is needed it will not contribute significantly to the overall power consumption.

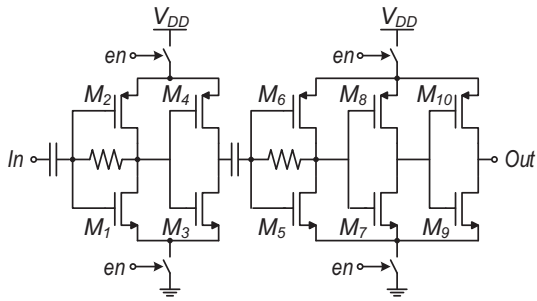


Figure 6.8 Schematic of the frequency divider buffer.

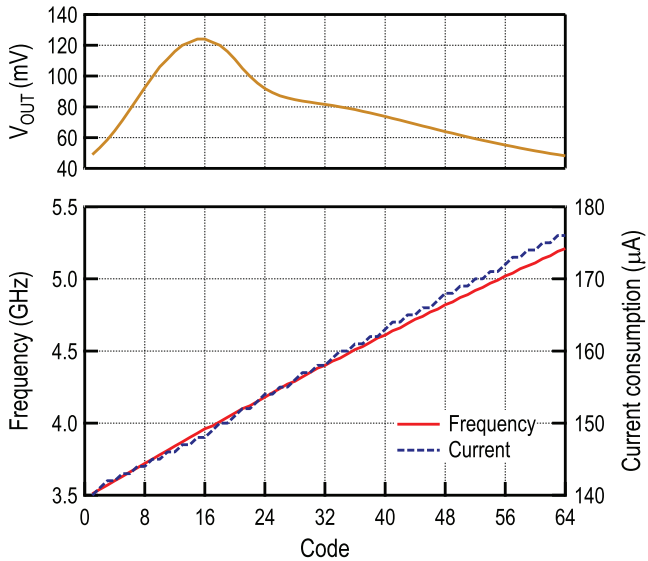


Figure 6.9 Simulated DCO frequency, current consumption and output voltage amplitude.

Figure 6.9 shows simulated frequency, current consumption and output amplitude of the designed DCO, including the two buffer inverters. Resonant load at the preamplifier input is used to boost the signal amplitude close to 4 GHz. The DCO covers the range from 3.5 GHz to 5.2 GHz, and with the 6 bit DAC, this results in frequency resolution of roughly 25 MHz. At 4 GHz, the DCO consumes 150 μW, for a 120 mV signal amplitude at the output. The linearity of the DCO is sufficient for the generation of the FM-UWB signal, and does not cause notable distortion in the output spectrum.

6.3.4 Preamplifier and Power Amplifier

The output stage of the transmitter consumes the largest portion of power and is therefore the most critical for the overall performance. As any other FM modulation, the FM-UWB is a constant envelope modulation, meaning that there is no need for use of special techniques such as outphasing, envelope elimination and restoration, adaptive biasing etc. However, low constraint in terms of output power (maximum output power is below -10 dBm), combined with large bandwidth of the FM-UWB signal, result in more complex output matching network, and consequently lower achievable efficiency.

Design of a power amplifier for low output power poses specific challenges, usually different than those seen in more common applications. Generally, for every power amplifier there is an optimal load impedance that results in highest efficiency for a given output power. Consider a PA that needs to provide 20 dBm output power. For a 50 Ω load this translates into a voltage swing of more than 6 V peak to peak. This becomes difficult to achieve in deep sub-micron technologies with a low supply voltage, and a matching network is required that will lower the load impedance to the optimal value, much smaller than 50 Ω. For the case of FM-UWB, the maximum output power is limited to -10 dBm, which translates into a 200 mV swing over a 50 Ω load. In this case, the optimal impedance seen from the PA needs to be higher than the load, and the matching network instead needs to boost the load impedance to maximize efficiency. This adds different constraints and changes the design approach compared to the first case. The second important difference between the high and low power PA design is in the driving circuits. At 20 dBm output power, driving circuits will consume only a small portion of the overall power, and will not affect the efficiency significantly. They become much more important when the output power becomes comparable to the consumption of the driving circuit and may greatly affect the choice of the PA class of operation.

In most mid and high power applications, with a constant envelope modulation, class E PA is commonly used as the most efficient solution. To achieve high efficiency, such PA requires a matching network precisely tuned to a certain frequency. Achieving high efficiency over a wide bandwidth (500 MHz in this case) becomes a difficult task with class E. Additionally, class E and other switching PAs have very high driving requirements, which pose problems for the driving circuits at low output power levels. For proper class E operation the switch needs to be driven with a full swing rectangular signal, with very short transition times, in order to minimize switching losses.

In addition, the efficiency of every switching PA is inversely proportional to the switch on resistance. This condition sets a limit to the minimum size of the PA transistor and consequently sets its input capacitance. Since the driver consumption is proportional to fCV_{DD}^2, at 4 GHz and -10 dBm output power, it will become comparable to the PA consumption, resulting in significant overall efficiency penalty. For this reason, linear power amplifiers are a better choice for this application.

For the proper choice of a linear PA, its efficiency must be taken into account together with the needed input signal amplitude. Going from class A to class C, the conduction angle of the PA decreases, and the efficiency increases. However, to maintain the same output power, the input signal must increase its amplitude at lower conduction angles, thus imposing higher driving requirements. Higher input amplitude means higher preamplifier consumption (proportional to the square of the amplitude). A good trade-off between driving requirements and PA efficiency is a class AB amplifier and is therefore used in this design.

As explained previously, for -10 dBm output power and 1 V supply, optimal impedance seen from the PA is proportional to V_{DD}^2/P_{out}, which is in this case much larger than 50 Ω [6, 7]. The matching network that will implement this ratio is difficult to implement on chip due to the limited quality factor and limited inductance value of the integrated inductors. The problem can be solved by lowering the supply voltage which consequently lowers the optimal impedance and the transformation ratio. Instead of using a separate circuit to lower the supply voltage, such as a DC-DC converter, the preamplifier and the PA can be stacked (similarly to the approach from [3]). At the same time, this simplifies the matching network, as the equivalent PA supply is reduced, and saves power since the preamplifier reuses the bias current of the PA.

The designed output stage, with the preamplifier and the main PA is shown in Figure 6.10. Capacitors C_{in1} and C_{in2}, together with the inductor L_{PPA} provide the resonant load for the DCO buffer in order to boost the amplitude around 4 GHz. Capacitor C_{in2} can be tuned to compensate for process variations. Bias current of the entire stage is determined by the bias point of the PPA transistor M_1. Just like the main PA, the PPA is also biased in class AB. Output power can be controlled by controlling the bias point of M_1. Filter that consists of the RF choke L_{PPA} and a decoupling capacitor C_{dec} provides a steady voltage at the source of M_2. Depending on the bias current this voltage will vary from 0.3 V to 0.4 V, and is determined by the V_{GS} of M_2 and M_3. The resonance frequency at the PPA output is determined by the L_{PPA} and the equivalent capacitance seen from the drain of M_1, which

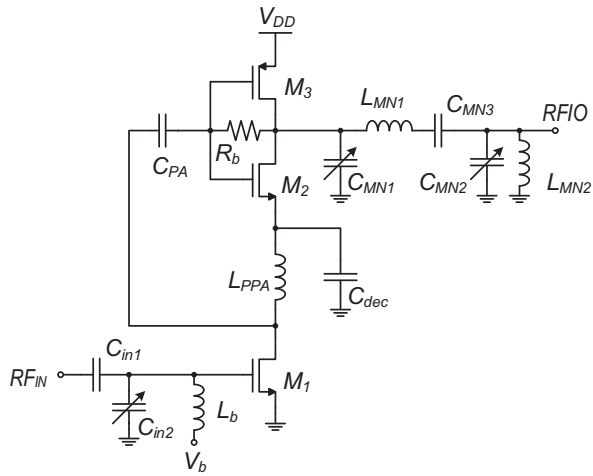


Figure 6.10 Preamplifier and power amplifier schematic.

is mainly determined by the C_{PA} and the gate capacitances of M_2 and M_3. The two resonant frequencies at the input and output of the PPA are offset from 4 GHz in opposite directions in order to provide a relatively constant signal amplitude at the PA input over 500 MHz bandwidth. The main PA is a complementary class AB power amplifier. It is self biased via a 95 kΩ resistor R_b. The PA input amplitude above 250 mV in the desired band is enough to drive the class AB amplifier in saturation and provide a relatively good efficiency. Output matching network that consists of inductors $L_{MN1,2}$, and capacitors C_{MN1-3} transforms the output 50 Ω impedance into roughly 700 Ω over the entire band of operation, as seen from the PA output. This is enough to provide an almost rail to rail signal at the PA output (with respect to the PA supply, meaning from 0.3 V to 1 V), that minimizes power dissipation in the two output transistors.

The output matching network is designed together with the matching network of the two LNAs. To simplify the overall design procedure, the LNA is designed to present a capacitive load at the RF IO in the off state. The total capacitive load at the RF IO is determined by the pad capacitance and the two LNAs. Since matching requirements are not the same in the receive and transmit mode, the matching network must be able to adjust to both. This can be achieved by adjusting the capacitance of C_{MN1} and C_{MN2}. The value of C_{MN1} changes from 120 fF to 520 fF in transmit and receive mode. The C_{MN2} is actually set to 0 in the transmit mode. Generally, the capacitance at

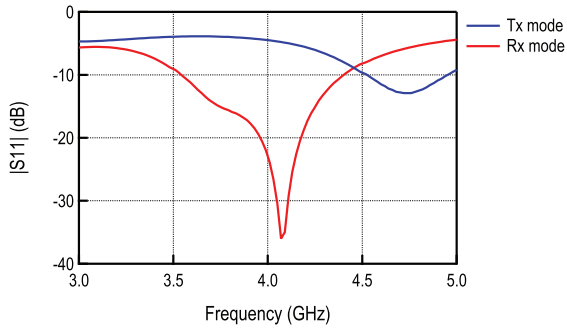
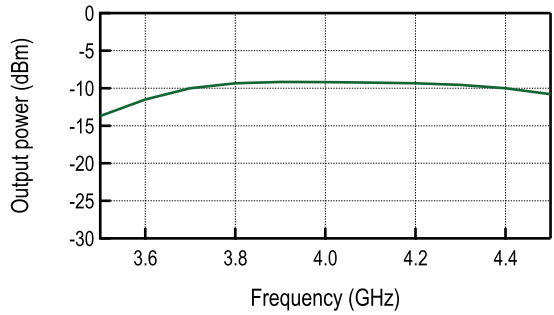


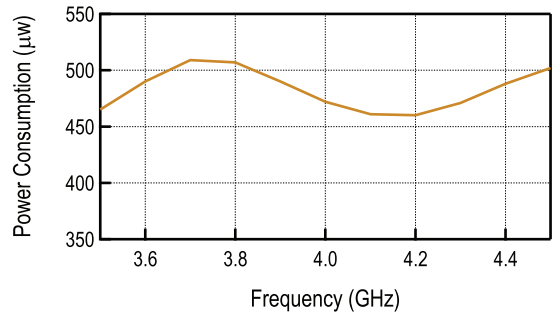
Figure 6.11 Simulated S_{11} parameter at the RF IO.

this node (RF IO) should be minimized in order to maximize the efficiency. Inductor L_{MN2} is placed to partially compensate this capacitance and to extend the bandwidth. In the receive mode, the value of C_{MN2} increases to 600 fF. In the actual implementation 3 bits are used to control the two capacitors, the first bit switches from transmit to receive state, and the additional 2 bits allow some frequency tuning, that allows small modifications of the resonance frequencies once the chip is placed on a PCB. Simulated S_{11} parameter at the RF IO port is shown in Figure 6.11 for the two modes of operation. It can be seen that in the transmit mode, the reflection coefficient is quite high, around -5 dBm in the band of interest, and would not provide adequate matching to a 50 Ω antenna. Once the capacitors are switched, the input reflection coefficient drops below -10 dBm from 3.6 GHz to 4.35 GHz.

Simulated output power, power consumption and efficiency of the output stage are shown in Figure 6.12. The shown characteristic of the PA is static in the sense that the signal frequency is constant. However, assuming a relatively slow moving FM-UWB carrier, the simulation should provide a good estimate of performance during transmission. The PA was designed to provide roughly constant output power over the desired frequency range of 500 MHz. The low equivalent Q factor of the output matching network results in lower peak efficiency of the amplifier, which is an inherent drawback of wideband power amplifiers, and the price to be paid for large signal bandwidth. As shown in Figure 6.12(a) the simulated output power varies less than 1 dB between 3.7 GHz and 4.4 GHz, with an average output power around -9.4 dBm. This level is somewhat higher than the allowed power in the UWB band. The design is intentionally targeting a higher output power since the actual power level is expected to be lower than the one simulated (due to losses on the PCB and imperfect matching). In the same band power consumption from a 1 V



(a)



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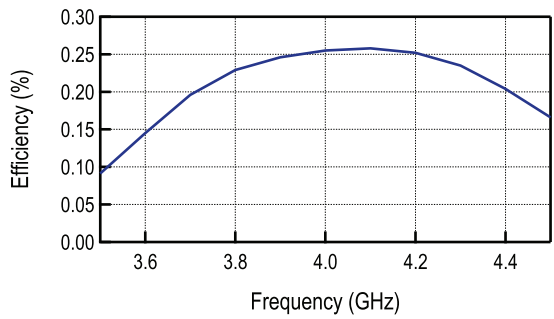


(c)

Figure 6.12 Simulated power amplifier output power (a), consumption (b) and efficiency (c) including the preamplifier.

supply varies between 510 μW and 460 μW, with an average value of 481 μW. The PA efficiency including the PPA is above 20% in the range of interest, with the average simulated efficiency of 24%. With the reported results, the proposed transmitter should consume the lowest amount of power of all the so far implemented FM-UWB transmitters.

6.4 Receiver Implementation

The two implemented receivers, MU and LP receiver will be described in detail here. The MU receiver is very similar to the receiver described in the previous chapter, only minor modifications are done at the circuit level. In the baseband, after the wideband FM demodulator, a channel filter and an FSK demodulator are added, so that the entire processing is now done on-chip. The same FSK demodulator is used by the LP receiver, however, in this case there is no need for the channel filter as only a single FM-UWB channel can be used.

6.4.1 RF Frontend

As in the previous case, the LNA and mixer are stacked (active mixer) to conserve power in both LP and MU receivers. The two schematics of the active mixer for the case of the MU receiver and the LP receiver are shown in Figures 6.13 and 6.14 respectively. Again, a transformer based approach is used to boost the equivalent transconductance of the input transistor to approximately $2G_{m1}$. As opposed to the previous version, there is no complementary input transistor, only the NMOS is used, which simplifies the layout of the LNA and reduces parasitics, however, the output bias point and the LNA gain are no longer decoupled. Switch, sw_1 is placed to disconnect the transformer when transceiver is in the transmit mode. This is done to avoid the impact of the transformer to the PA output impedance and efficiency degradation. Resistors R_{M1-4} are fixed to 15 kΩ, no gain switching is present in this design, although G_{m1} can be varied by slightly tuning the bias current.

The LP RF frontend only has a single differential output, and therefore only needs one LO input. This allows to simplify the oscillator and save power in the the LO generation. Although a single LO signal is present, mixing is done using a current steering differential pair $M_{M1}-M_{M2}$, where gate of M_{M2} is tied to V_{bm}. Because a single-ended LO signal is used, voltage gain will be lower and noise figure will be higher compared to a case with a differential driving signal with the same amplitude. Load of the LP mixer is done using PMOS transistors M_{M3} and M_{M4}, that provide the output bias point and load resistors R_{M1} and R_{M2} that determine the output impedance, allowing some decoupling between the two.

Input matching network is implemented in the same way for both frontends. The input reflection coefficient is given in Figure 6.11, and is the same for both (although there is a small difference in G_{m1}). The MU

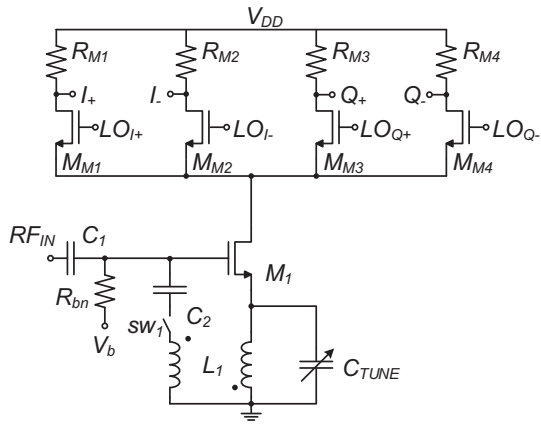


Figure 6.13 MU receiver LNA/mixer schematic.

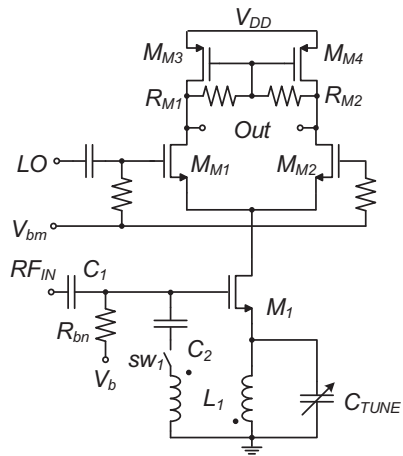


Figure 6.14 LP receiver LNA/mixer schematic.

LNA/mixer provides 13 dB differential voltage gain, together with a noise figure of around 15 dB, while consuming 100 μW. The LP LNA/mixer achieves 11 dB gain and 19 dB noise figure (it should be noted that a single ended LO signal of a lower amplitude is used) while consuming 70 μW. In both MU and LP implementation the main source of noise is transistor M_1. For both active mixers the input referred 1 dB compression point is around $P_{1dB} = -16$ dBm, and the third order intercept point is around $IIP_3 = -3$ dBm.

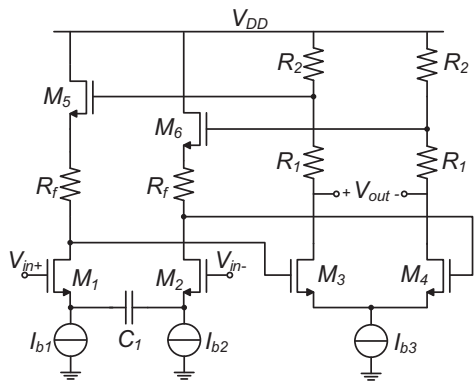


Figure 6.15 IFA schematic of MU and LP receiver.

6.4.2 IF Amplifiers

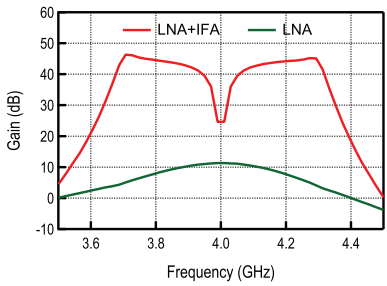
A Cherry-Hooper amplifier described in the previous chapter was reused in this design. First difference that can be noticed compared to the previous design is that the capacitor C_1, used to prevent offset propagation, is now placed in the source of the first differential pair. The second difference is that resistor R_f is now used to provide gain switching. It was established by simulation that additional parasitics due to switching circuitry at R_f have less impact on the amplifier bandwidth than was the case previously. A single gain control bit is provided per stage, resulting in 3 control bits for the 3 cascaded IF stages, that provide gain switching in roughly 5 dB steps. As in the previous case, lower gain setting slightly extends bandwidth.

Although schematics of the two, LP and MU, IF amplifiers are identical, values of different circuit elements are different in order to conform to slightly different design requirements. Output resistors are slightly lower in the two last stages of the IF amplifier in order to cope with the higher capacitive load at this node. The capacitive load is mostly due to the buffers that precede the wideband FM demodulators. Additional difference exists in the LP IF amplifier and is concerning the capacitor C_1. Namely, in the LP receiver case, the IF amplifier is also part of the FM demodulator, and acts as a frequency discriminator (performs FM-AM conversion). The high pass frequency characteristic needed for demodulation is implemented using a small capacitor C_1. The zero and pole coming from this capacitor are given by

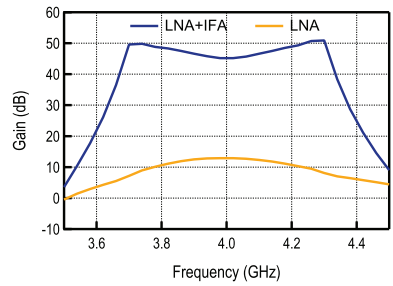
$$z \approx -\frac{1}{2C_1 R_{o,b}}, \quad p \approx -\frac{G_{m1}}{2C_1}, \tag{6.2}$$

where $R_{o,b}$ is the output resistance of the tail current source. The approximation is valid if $G_{m1}R_{o,b} \gg 1$. The cut-off frequency of the high-pass filter is determined by the M_1 transconductance and the source capacitor. This small capacitor of 200 fF is placed at the third stage of the IF amplifier. Large capacitors of 2.5 pF used for the first two stages provide a cut-off frequency below 5 MHz and should not have a significant impact on demodulation. Finally, the chosen values result in a first order high pass characteristic with the cut-off frequency above 200 MHz.

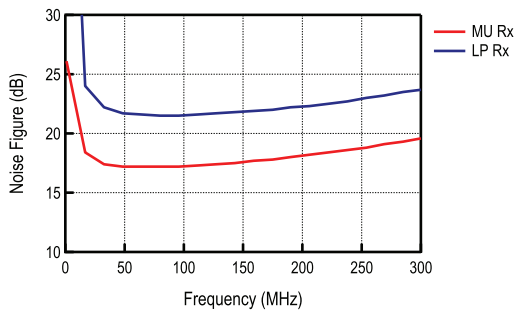
Simulated characteristics of the implemented amplifiers are shown in Figure 6.16. The high-pass characteristic of the IF amplifier in the LP receiver provides the FM-AM conversion before the envelope detector. In the pass band the IF amplifier provides more than 35 dB of gain, which together with the RF frontend results in the conversion gain of around 45 dB. The MU receiver IF amplifier provides around 40 dB gain, resulting in almost 50 dB conversion gain together with the RF frontend. Both amplifiers provide more than 300 MHz bandwidth, that should be enough to compensate for the ± 50 MHz carrier frequency offset. Sharp, 6th order filtering characteristic



(a) LP Rx frontend gain.



(b) MU Rx frontend gain.



(c) Frontend noise figure for MU and LP Rx.

Figure 6.16 Simulated characteristics of the LP and MU Rx frontend.

provides good rejection of out of band interferers. The total noise figure of all the stages preceding the demodulator is around 22 dB for the LP receiver and around 18 dB for the MU receiver. The limited gain of the LNA/mixer stage, results in increase of the noise figure due to the noise of the IF amplifiers. Higher noise in the LP IF amplifier is coming purely from the RF frontend. Together with the 6 dB difference in sensitivity, coming from the demodulator implementation, the 4 dB difference in noise figure should amount to roughly 10 dB difference in sensitivity between the two receivers. In this case, this sensitivity loss is a price to pay for low power consumption. In both cases, a single IF stage consumes around 20 μW, amounting to a total IF power consumption of 60 μW in the case of LP, and 120 μW in the case of MU receiver.

6.4.3 Receiver DCO

The quadrature DCO described in the previous chapter was reused in the MU receiver without any significant changes. Since the LP receiver does not require quadrature LO signals, a different DCO was designed, allowing to save power needed to generate the LO signal. Knowing that the DCO is one of the biggest consumers in the receiver, such an approach allows to further reduce the overall power consumption of the LP receiver.

The implemented LP DCO is shown in Figure 6.17. The architecture presented here uses the concept from [8] to lower the DCO consumption. The ring oscillator itself (transistors M_{7-11}) oscillates at one third of the

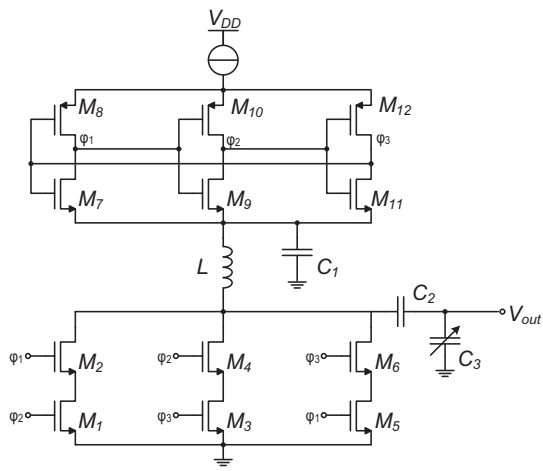


Figure 6.17 LP receiver DCO schematic.

desired frequency. The three phases ϕ_{1-3} are then combined using an edge combiner (transistors M_{1-6}) in order to multiply the output frequency by 3. The oscillator and the edge combiner are stacked on top of each other and reuse the same current. The two stages are separated by an LC filter that provides a stable voltage for the source of the ring oscillator NMOS transistors on one side, and high impedance for the combiner output on the other. The stable source voltage sets at approximately 0.35 V and does not change significantly with the oscillation frequency. The resonance frequency at the edge combiner output is set by the values of the inductor L and the capacitor C_3, and can be tuned by switching the capacitor bank C_3. The edge combiner acts at the same time as the LO buffer in the sense that a change of the load capacitance at its output does not affect oscillation frequency (in the first order approximation). No additional buffers are added before the mixer and frequency divider input. Oscillation frequency is controlled via the supply current of the ring oscillator. One downside of the chosen DCO implementation is the fact that output amplitude and oscillation frequency cannot be set independently. The oscillator bias current, is at the same time bias current of the frequency trippler and therefore also sets the output amplitude. As a consequence, the output amplitude is lower than in the case of the MU oscillator resulting in lower mixer conversion gain and hence in a higher noise figure.

Simulation results of the designed oscillator-trippler are shown in Figure 6.18. The oscillator covers a range from 3.5 GHz to 5 GHz, which for 6 control DCO bits corresponds to a resolution of around 25 MHz. At the same time power consumption varies from 57 μW to 88 μW. At 4 GHz the oscillator is expected to consume 65 μW from a 1 V supply. At this power consumption the DCO output amplitude is equal to 85 mV. As it can be seen in Figure 6.18, the amplitude is highly dependent on the resonance frequency of the output LC network, which was not the case in the MU DCO that provides an almost constant amplitude over the entire frequency range. The tuning capability is added, in order to compensate for process variations and precisely tune the resonance frequency and maximize the output amplitude at 4 GHz after production.

6.4.4 Demodulator

The demodulator of the MU receiver, shown in Figure 6.19, is similar to the previously implemented demodulator. The only difference is the load of the double balanced mixer, that here has a band-pass characteristic

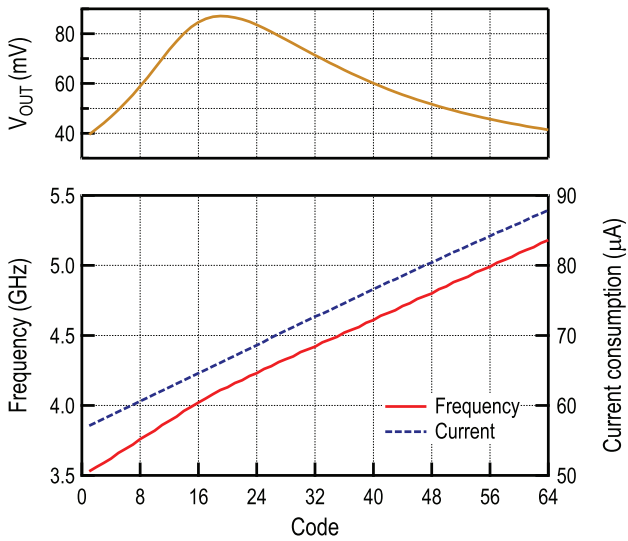


Figure 6.18 LP receiver DCO simulated frequency, current consumption and output voltage.

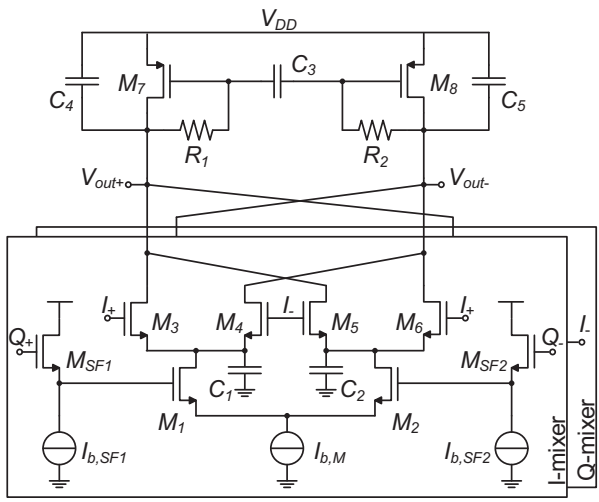


Figure 6.19 MU receiver demodulator schematic.

instead of a low-pass characteristic. In principle, this should improve the suppression of narrowband interferers. After the first FM demodulation the narrowband interferer should be located at very low frequencies, determined by the signal bandwidth, that should be filtered out. Capacitor $C_4(5)$ attenuates components at frequencies higher than 2.5 MHz, and doesn't

play a role below 1 MHz. Disregarding this capacitor the mixer load impedance is given by

$$Z_{out} = \frac{1}{G_{m7}} \frac{1 + 2sR_1C_3}{1 + 2sC_3/G_{m7}}. \tag{6.3}$$

At low frequencies, the mixer output impedance will be low, and equal to $1/G_{m7}$, thus attenuating potential interferers. At frequencies above the high-pass cut-off frequency $\omega_H = G_{m7}/2C_3$, the impedance seen from the mixer increases to R_1, providing higher voltage gain.

The LP demodulator consists of the frequency discriminator and the envelope detector. The frequency discriminator is implemented as a high-pass filter and is a part of the IF amplifier. The envelope detector is shown in Figure 6.20. The circuit is essentially a double balanced mixer, where the input signal is mixed with itself. To provide the two different bias points for the two mixer inputs, two different source followers were used. Source followers $M_{SF1,3}$ use native NMOS transistors with a 0 threshold voltage and drive the first mixer input (transistors M_{3-6}). Lower bias for the second mixer input (transistors $M_{1,2}$) is provided by the low threshold voltage devices $M_{SF2,4}$. The bias currents are the same for all the source follower stages. For the load of the mixer, the same approach is used as for the MU demodulator, with the difference that the pass-band is set from 2 MHz to 2.5 MHz. This is done because the LP demodulator doubles the frequency of the sub-carrier signal. Since the transmit SC channel is centered at 1.05 MHz, the received sub-carrier signal is located at 2.1 MHz.

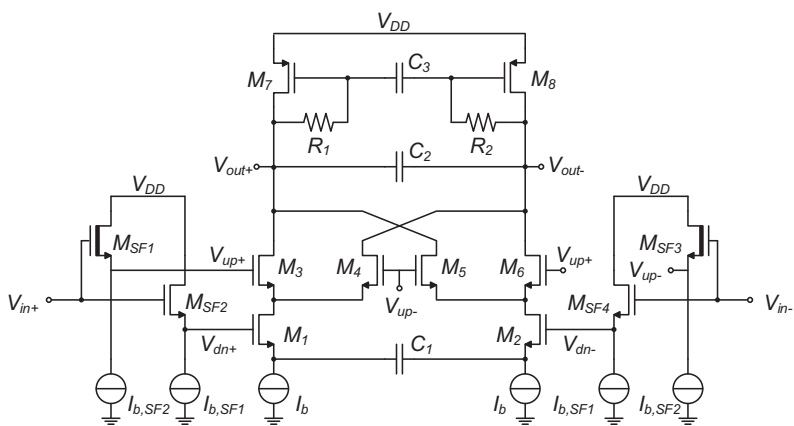


Figure 6.20 LP receiver demodulator schematic.

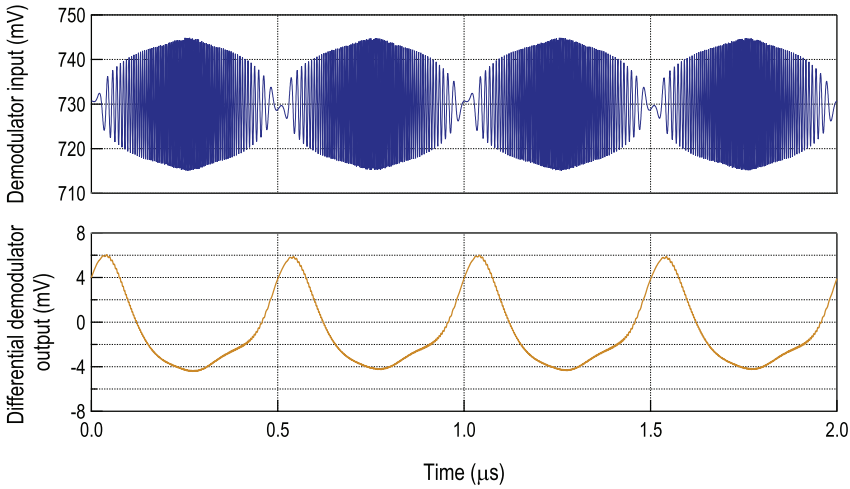


Figure 6.21 LP receiver demodulator input and output waveforms.

Simulated waveforms of the demodulator input and output signal are shown in Figure 6.21. The effect of the high-pass characteristic of the IF amplifier can be observed in the input signal as the low frequency components are highly attenuated. After self mixing, the high frequency components disappear, and only envelope is left at the output. The output pulses appear at twice the transmitted SC frequency. After passing through the low-pass filter that follows the demodulator, higher components are attenuated and signal resembles a sine wave at the comparator input.

6.4.5 N-Path Channel Filter

The output of the first FM demodulator is the FSK modulated sub-carrier signal. Depending on whether one or several transmitters transmit simultaneously, there may be one or more sub-carrier signals present at the demodulator output. The purpose of the channel filter is to amplify the desired channel and filter out all the interfering sub-channels. As explained previously, the implemented receiver targets 4 sub-channels, each 200 kHz wide, with 300 kHz separation between adjacent channels. The implemented receiver is targeting a maximum of 10 dB difference in power levels between the two input FM-UWB signals. This translates into 20 dB difference in power of sub-channels after the first FM demodulator. To provide sufficient SNIR (signal to noise and interference ratio) before the FSK demodulation, the

filter should attenuate the interfering sub-channels by 40 dB, thus providing the desired signal 20 dB stronger than the interferer. This chosen constraint is somewhat more stringent than necessary in order to provide margin for slight performance degradation compared to simulations. The filter should therefore provide a 200 kHz pass-band, and attenuation of 40 dB at 250 kHz away from the center frequency. Furthermore, the filter must be tunable from 1 MHz to 2.2 MHz in order to cover the entire sub-carrier range.

N-path filters seem like an excellent candidate for the given specification as they are known for their wide tuning range and high quality factor. The principle of N-path filters has been known for a long time [9], but they gained significant popularity in recent years as an alternative solution for high-Q RF filters that does not require off-chip passive components. Typical N-path filter consists of N parallel branches, each of them containing a switch and a capacitor in series. By driving the switches with N non-overlapping clock phases with frequency f_{ck}, the structure acts as a band-pass filter with a center frequency f_{ck}. This can be seen as a low-pass to band-pass transformation of the filter made of the input resistance and the N aforementioned capacitors. The achievable Q-factor can be very high and is proportional to the RC constant, the number of phases used and the clock frequency [9–11]. There are some downsides to N-path filters, that are generally present in all sampling systems. First one is that the pass-band also appears at the integer multiples of the clock frequency. An improvement can be obtained by connecting the capacitors differentially, which removes all the even harmonics. The remaining harmonics still need to be filtered out by another filter following the N-path filter. The second downside is folding of signal and noise around frequencies that are multiples of $N f_{ck}$ (aliasing). This issue is typically solved by introducing an antialiasing filter that precedes the N-path filter, just like it is done with any sampling system (e.g. ADC). Fortunately, in this particular application noise is not an issue as this filter is close to the end of the receiving chain.

N-path filters have been used in many receivers, and have been proven to provide good linearity and interference rejection [12–15]. However, in all these implementations N-path filters act as a high-Q second order filter, with a very narrow pass-band (relative to the center frequency). In this application, a relatively flat pass-band characteristic is required, along with a linear phase, in order to avoid distortion of the sub-carrier signal. Ideally, this requires translation of a higher order equivalent low-pass filter to the desired center frequency. The described design has been demonstrated for RF frequencies in [16–18], here it is reused and adapted for low frequency and low power operation.

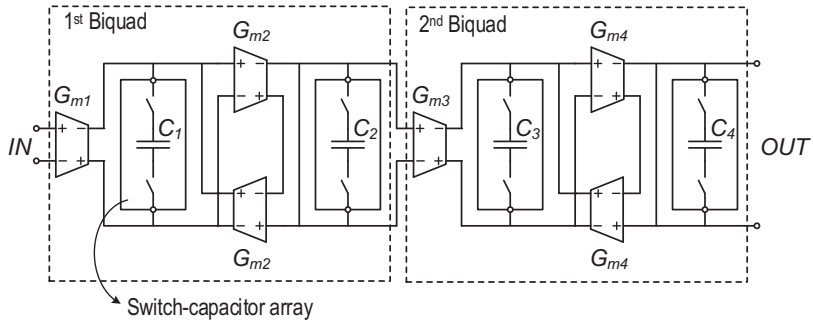


Figure 6.22 Band-pass N-path filter schematic.

The implemented N-path filter is presented in Figure 6.22. It is immediately clear that if the switches are removed, the shown filter becomes a standard low-pass $\mathrm{G_m}-\mathrm{C}$ filter. In fact, it was shown in [18] that by adding switches, and scaling the capacitor values by the number of phases, such that $C_x = C_{BBx}/N$, the low-pass characteristic translates into an equivalent band-pass characteristic. This characteristic will be affected by the non-idealities such as switch resistance and parasitic capacitance. The parasitic capacitances will result in slight asymmetry around the filter center frequency. It is possible to compensate for the effect of the parasitic capacitances by adding feed-forward capacitors [18]. In this case, it is not necessary to add the compensation capacitors as the parasitics are relatively small compared to the actual filter capacitors due to narrow filter bandwidth and low frequency of operation. Switch resistance affects the quality factor of the filter and limits the attenuation in the stop-band. This is an important problem at RF, as the filter is typically driven by a $50\,\Omega$ source, since the maximum attenuation is limited to

$$A_{at,max} = \frac{2R_{sw}}{R_{in} + 2R_{sw}}, \tag{6.4}$$

where R_{in} is the source resistance, and R_{sw} is the switch resistance, factor 2 is present in differential implementation, since two switches are used. In order to achieve the desired attenuation, switch resistance must be sufficiently low (much smaller than $50\,\Omega$). This constraint will dictate the size of the switch and the driving requirements, and consequently power dissipation of the clock network. In this application, however, the filter is driven by an OTA with a high output resistance, on the order of $20\,\mathrm{k}\Omega$, which enables use of relatively small switches, and low power consumption.

The filter design procedure is done in two steps. First, a low-pass equivalent filter is designed, with a 100 kHz pass-band, and 40 dB attenuation at 250 kHz. In the second step, switches are added, and capacitors are scaled in order to obtain the desired 200 kHz pass-band characteristic around the center frequency. In other applications it might also be necessary to add feed-forward capacitors to compensate for the parasitics. For this design, it was determined that a 4th order, type 1 Chebychev transfer function satisfies the given specifications. Two biquadratic sections are used to implement the network with 4 poles p_{1-4}. The low-pass equivalent transfer function of each biquadratic section is given by

$$H(s) = \frac{H_0}{as^2 + bs + 1}, \tag{6.5}$$

$$H_0 = \frac{G_{m1}G_{m2}}{G_{m2}^2 + G_{o1}G_{o2}}, \quad a = \frac{C_1C_2}{G_{m2}^2 + G_{o1}G_{o2}},$$

$$b = \frac{C_1G_{o2} + C_2G_{o1}}{G_{m2}^2 + G_{o1}G_{o2}}, \tag{6.6}$$

where G_{o1} is the output conductance at the output of G_{m1}, and G_{o2} is the output conductance at the input of G_{m3}. The active filter can also provide some voltage gain. Assuming that $G_{m1}G_{m2}/G_{o1}G_{o2} \gg 1$, gain can be approximated as $A_v = G_{m1}/G_{m2}$. Coefficients a and b are determined by the two poles

$$a = \frac{1}{p_1p_2}, \quad b = \frac{p_1 + p_2}{p_1p_2}, \tag{6.7}$$

for the first biquadratic section, and in the same way, using p_3 and p_4, for the second biquadratic section. Once the coefficients a and b are set, parameters G_m, G_o and C must be chosen. The transconductances $G_{m1,2}$ are limited by the power consumption constraints that limit the bias current of each transconductor. Transconductors are implemented using a Krummenacher differential pair [19], as shown in Figure 6.23, in order to provide better linearity. Transistors of the differential pair are biased in weak inversion, with $\beta_1/\beta_3 = 2$, corresponding to the minimum ripple condition. With 4 μA per differential pair, the equivalent transconductance is set to 40 μS. Output resistance of each cell (R_1 from Figure 6.23), and capacitors $C_{1,2}$ are then determined to implement the desired transfer function. Finally, the chosen capacitance values are scaled by factor N, which corresponds to the number of phases.

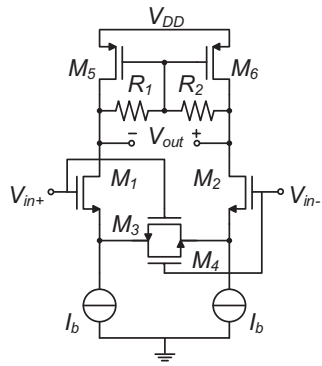


Figure 6.23 Transconductor of the N-path filter.

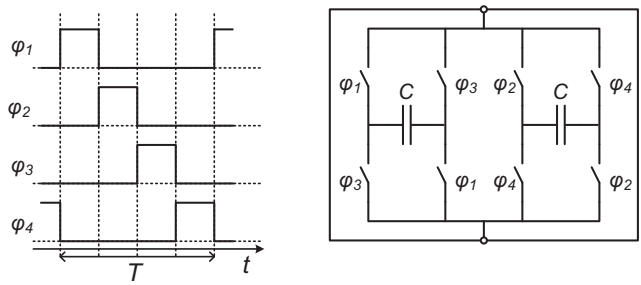


Figure 6.24 Non-overlapping clock phases used to drive switches and the differential switch-capacitor array.

In this design, four phases are used. The driving signals, and the switched-capacitor array are shown in Figure 6.24. Differentially connected capacitors cancel out the even harmonics. Using more phases would allow slightly better performance and less noise folding, but would increase the number of switches, and power consumption. Furthermore, four non-overlapping phases, can be generated using an input clock at four times the filter center frequency. In this case, it is convenient since the same clock can be used by the FSK demodulator. The circuit that generates different phases ϕ_{1-4} is shown in Figure 6.25. The three flip-flops divide the input clock by 4 and provide four equally spaced phases with a 50% duty cycle. The desired waveforms are then produced by the four AND gates.

Finally, the simulated filter characteristic is shown in Figure 6.26. In the simulation, 5 MHz input clock is used, resulting in center frequency of

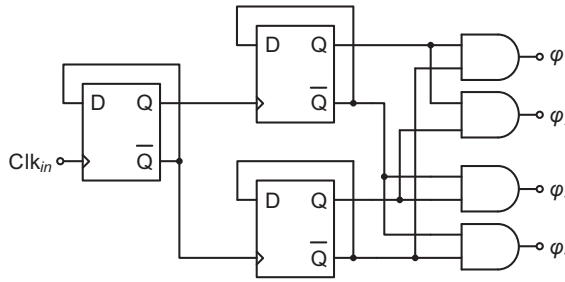
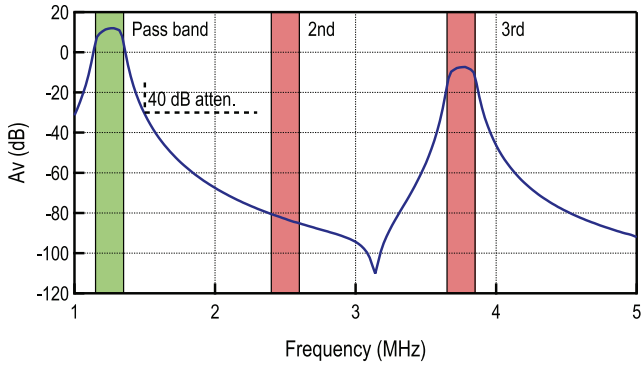
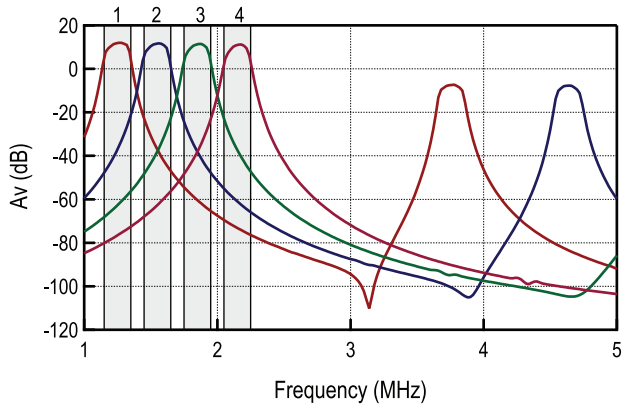


Figure 6.25 Non-overlapping clock generator.



(a) Channel 1.



(b) All four channels.

Figure 6.26 Transfer function of the N-path filter.

1.25 MHz. As explained previously, the differential capacitors cancel out all the even harmonics, and so the first higher order harmonic appears at 3.75 MHz. This is off-course the idealized case, and the attenuation of second harmonic will be limited by the component matching. Slight asymmetry around the center frequency can be observed, as expected, but in this case it does not cause severe distortion of the FSK signal. The filter center frequency can easily be tuned by adjusting the input clock frequency. Furthermore, bias currents of the transconductors can also be adjusted to modify the gain, filter bandwidth and attenuation in the stop-band.

6.4.6 LF Amplifier and Comparator

The low frequency (LF) amplifier, placed before the comparator, filters out high frequency noise, and amplifies the signal to the level needed by the comparator. The same architecture is used in both MU and LP receivers, with the pass-band adjusted to the desired frequency range. In the MU receiver, this filter also attenuates the 3rd harmonic of the N-path filter transfer function. A cascade of two fully differential amplifiers is used. A single amplifier cell is shown in Figure 6.27, together with the small signal model of the half circuit. Each amplifier actually implements a 2nd order transfer function. The idea to use a negative resistance to implement the second order function was found in [20, 21]. This approach also allows a high quality factor, using a negative resistance that cancels out the real part of the output impedance, however,

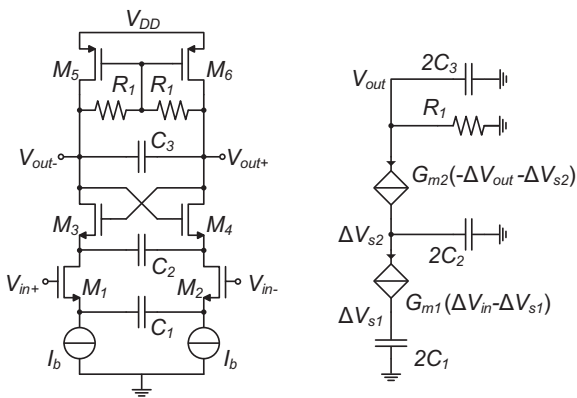


Figure 6.27 Schematic of the second order cell of the LP filter and half circuit small signal schematic.

one must be careful to maintain the circuit stable and avoid oscillations. The voltage gain is given by

$$A_v(s) = \frac{s\,2C_1G_{m1}G_{m2}R_1}{(G_{m1}+s2C_1)} \times \frac{1}{(G_{m2}+s(2C_2+2R_1G_{m2}(C_3-C_2))+s^2 4C_2C_3R_1)}. \quad (6.8)$$

The zero and pole created by C_1 provide the high-pass part of the characteristic that filters out flicker noise together with any low frequency components. The second factor in the denominator provides the 2nd order low-pass filtering. If the first real pole is sufficiently far from the two complex poles, gain in the pass band will be given by

$$A_{v,pb} \approx G_{m1}R_1. \quad (6.9)$$

For the two poles generated by this factor to be in the left half-plane, the coefficient with s must be positive. The circuit remains stable as long as $2C_2 + 2R_1G_{m2}(C_3 - C_2) > 0$. This will be guaranteed if the capacitor C_3 is larger than the capacitor C_2. Otherwise, given the sufficiently high bias current, and consequently the transconductance G_{m2}, the circuit might start to oscillate.

The simulated frequency characteristics of the two LF amplifiers are given in Figure 6.28. The frequency band is selected based on the expected sub-carrier frequency. Since a larger band is needed for the MU receiver, in order to accommodate multiple SC channels, gain is slightly lower, around 25 dB in the pass-band, compared to approximately 32 dB in the LP receiver

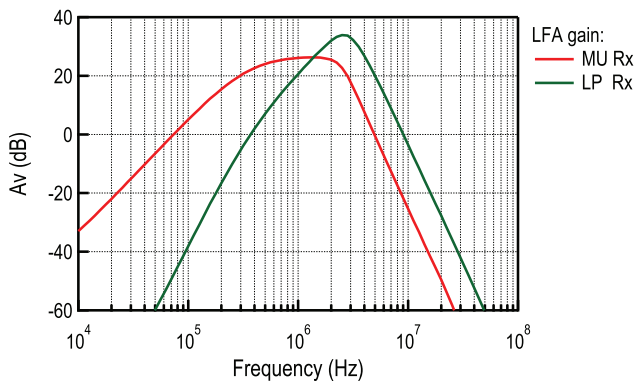


Figure 6.28 Simulated frequency characteristic of the MU and LP receiver LFA.

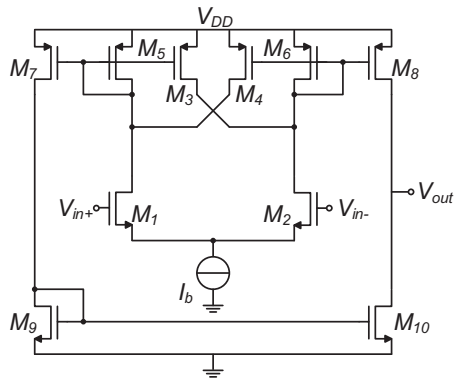


Figure 6.29 Comparator schematic.

path. In this case, linearity is not a concern, since only a single FSK signal is expected at the input (additional FSK signals should be removed by the preceding channel filter).

Comparator following the LF amplifier acts as a limiter and provides a rail-to-rail output signal that is needed for the digital FSK demodulator. The schematic of the comparator is shown in Figure 6.29. It is designed to provide full swing for an input sine signal with a minimum differential amplitude of 20 mV at up to 5 MHz (which is above the needed range). The core of the comparator are transistors M_{1-6}. In order to provide better performance and avoid glitches due to noise, a small hysteresis is introduced in the comparator characteristic, on the order of 10 mV. This is done using the positive feedback transistors M_3 and M_4. Assuming the transistors are operating in weak inversion, the difference between the two threshold voltages is given by

$$\Delta V_{TH} = 2\mathrm{nU_T} \ln k, \tag{6.10}$$

where factor k is defined as $k = \beta_3/\beta_5 = \beta_4/\beta_6$. Transistors M_{7-10} are added to provide a full swing output signal compatible with CMOS logic. The comparator consumes between 5 μA and 10 μA, depending on the bias current setting. Since the expected input voltage amplitude is supposed to be larger than 20 mV, offset constraints are easily achievable and no calibration is necessary.

6.4.7 FSK Demodulator and Clock Recovery

The last block in the system is the FSK demodulator, that is implemented together with the clock recovery circuit. The demodulator implemented here

must be able to demodulate an FSK signal with the modulation index of 1, or equivalently 50 kHz frequency deviation at a data rate of 100 kb/s. The FSK demodulator reported in [3], is very simple, and consumes a small amount of power, but requires a large frequency deviation (250 kHz deviation was used). In this case, in order to support multiple sub-carrier channels, frequency deviation is limited to 50 kHz, and a different approach is needed.

The proposed demodulator, shown in Figure 6.30 is a digital version of the delay line demodulator. The input signal is first sampled using a clock whose frequency is four times higher than the FSK signal center frequency. The same clock is used for the N-path channel filter. By adjusting the reference clock frequency, the corresponding sub-channel is selected. The sampled signal is then demodulated using a delay line and a "mixer". Sampling the signal allows to implement the delay line as a chain of flip-flops controlled by the same reference clock. Delay can be configured easily by controlling the number of flip-fops in the signal path, which is simply achieved by configuring the multiplexers. This allows a more elegant control compared to analog solutions such as RC delay networks. An XOR gate plays the role equivalent to the mixer in the analog demodulator implementation. Depending on the delay, and whether the input frequency is higher or lower than the reference clock frequency, the output of the XOR gate will be '1' or '0'. Simulated signal at the FSK demodulator output is shown in Figure 6.31(a). Since the output signal is not perfectly clean (even without the presence of noise), it cannot be simply sampled, instead it is first filtered using a windowed accumulator. In each clock cycle, the accumulator output is either incremented or decremented depending on the XOR output. The accumulator output is then used to make a decision for the output bit and to recover the symbol clock.

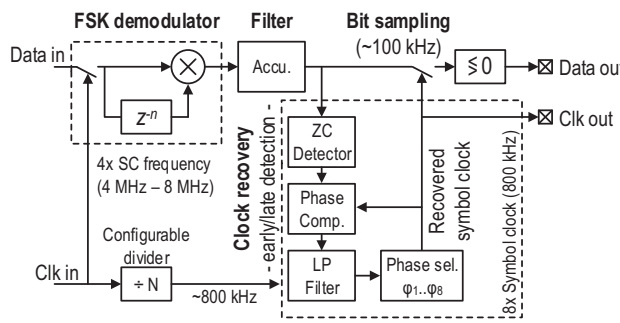
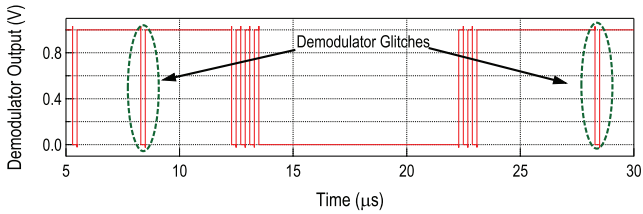
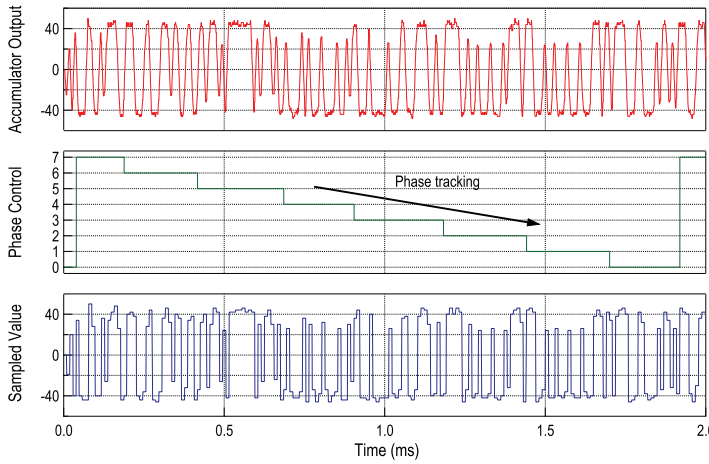


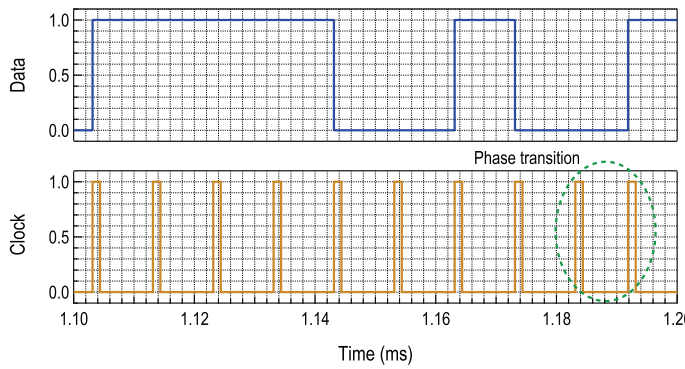
Figure 6.30 Block diagram of the FSK demodulator and clock recovery circuit.



(a) FSK demodulator output signal.



(b) Internal signals of the clock recovery circuit.



(c) Output signals.

Figure 6.31 Simulated signals of the FSK demodulator and clock recovery circuit.

A clock recovery circuit is a necessary block in any receiver, and has a particularly important role here. As previously discussed, one of the good properties of FM-UWB is the inherent robustness to frequency offsets. Mismatch in carrier frequency of several megahertz, or even tens of megahertz will not cause a significant performance penalty. However, for the whole receiver chain to work properly, the baseband must also be able to tolerate a certain frequency offset. This is accomplished via a dedicated circuit that tracks the transmit symbol clock and adjusts the clock frequency on the receiver side. The amount of frequency offset that must be tolerated depends on the implementation of the reference oscillator. One of the aims of this work is to demonstrate the feasibility of a fully integrated transceiver, which would include the reference oscillator. This also means removing the external crystal reference and minimizing the number of off-chip components. Unfortunately, the integrated RC oscillators cannot achieve the performance of a crystal oscillator, and the precision of the reference frequency will be much worse, in the order of thousands of ppm instead of tens of ppm. By using the FM-UWB, this relatively large frequency variation can be allowed, assuming that the clock recovery circuit can compensate the frequency offset between the transmitter and the receiver. Recently, integrated RC oscillators achieved precision that is in the order of ± 2500 ppm across the designated temperature range [22–25], which is a range that can be easily covered by the clock recovery circuit shown here.

The implemented clock recovery is based on a simple early/late zero crossing detection. The clock used for this circuit is derived from the reference clock, with the average frequency 8 times higher than the symbol rate, that is 800 kHz. This clock is then used to generate 8 different phases of the symbol clock, one of which is used to sample the accumulator output at a correct time instance. The clock recovery circuit determines which phase is used and works in the following way. First a zero crossing is detected from the accumulator output. In order to avoid false crossings due to noise, the circuit needs to detect a sufficient difference in levels between several consecutive samples. The phase comparator then determines whether the current zero crossing is early or late with respect to the currently selected clock phase. Depending on the number of clock cycles between the zero crossing and the reference, the corresponding value will be added to or subtracted from the register value of the LP filter (here the LP filter is simply implemented as an accumulator). Once the register value increases or decreases past a defined point, an up or down phase shift occurs. Depending on the frequency offset between the transmitter and the receiver, phase shifts will occur more or less often. As the phase changes, so does the average frequency of the receiver

symbol clock. As long as the circuit is able to track symbols, this average frequency should correspond to the transmitter symbol clock frequency. The speed of the control loop can be controlled through the LP filter coefficient, that directly determines the filter bandwidth. Increasing the coefficient allows the loop to track larger difference in frequencies, but also makes it more prone to errors due to noise.

An example of the clock recovery circuit operation is given in Figure 6.31(b). In this case, the transmitter reference frequency is 2000 ppm faster compared to the reference on the receiver side. One can notice that the phase control signal constantly decreases (until 0 at which point it goes back to 7), which results in the average frequency of the symbol clock below the reference frequency. An example of the phase shift is shown in Figure 6.31(b). In that particular time instance the instantaneous frequency of the symbol clock frequency drops to 7/8 of the reference frequency during one cycle. The maximum theoretical frequency offset that can be tracked, assuming a phase shift occurs in every cycle, is $\pm 1/8$ of the reference frequency.

6.4.8 SAR FLL Calibration

Ring oscillators used to generate the LO signal in the receiver and the FM-UWB signal in the transmitter consume a small amount of power, but are sensitive to process, voltage and temperature variations. For that reason they need to be calibrated periodically to maintain frequency offset within certain limits. It was shown in the previous chapter that a relative frequency offset of ± 50 MHz between the receiver and transmitter causes only a minor performance degradation, and beyond that limit sensitivity decreases rapidly. Depending on the rate of environmental changes, the oscillators will need to be calibrated once every few hours, or potentially days.

Calibration is performed using an on-chip SAR FLL, shown in Figure 6.32. Configuration of each oscillator is controlled using one of the two registers, one set manually by the SPI, and the other set by the calibration loop. The number of cycles for calibration is equal to the number of register bits used to set the DCO frequency. In each cycle one bit is set. Once the bit is set, the oscillator frequency is measured and compared to a reference value, if it is higher, the bit is set back to '0', otherwise it remains '1'. The DCO frequency is measured using two counters. The first counter counts the number of reference clock cycles up to value $N_{f,ref}$ that determines the duration of the measurement interval as $T_{ref}N_{f,ref}$. During that interval, the second counter counts the number of cycles of the frequency divider output N_{cnt}. This value is then compared to the reference value N_{ref} in order to determine

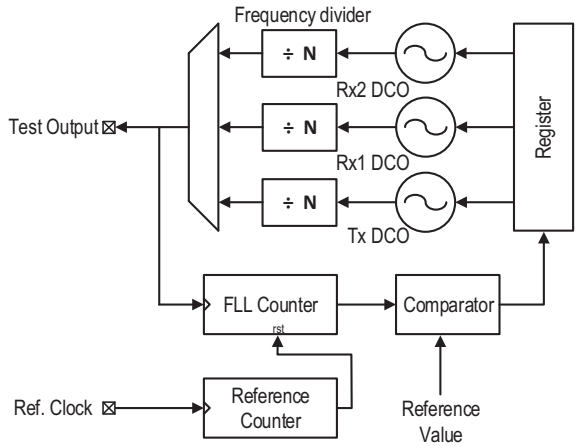


Figure 6.32 SAR FLL block diagram.

whether the corresponding bit should be '0' or '1'. Finally, assuming infinite resolution (number of bits or equivalently cycles), the frequency of the DCO after calibration will be given by

$$f_{DCO} = N_{div} f_{div} = N_{div} \frac{N_{ref}}{N_{f,ref}} f_{ref}, \tag{6.11}$$

where N_{div} is the frequency divider ratio (providing values between 128 and 1024) and f_{div} is the frequency at the divider output. In reality, the DCO configuration will produce the highest frequency that is still below the frequency given by Equation 6.11. The frequency resolution of the FLL depends on the duration of the measurement interval and the division ratio $\Delta f = f_{ref} N_{div} / N_{f,ref}$. The only requirement here is to maintain the FLL resolution below the DCO resolution, that is in the order of 25 MHz.

An example of a measured calibration cycle is presented in Figure 6.33. The measurement is done using the frequency divider output signal at the test port. For the shown measurement, reference clock frequency is set to 4 MHz, and $N_{div} = 1024$, $N_{f,ref} = 1024$ and $N_{ref} = 1000$. After 6 steps of calibrations, 6 DCO control bits are set. The resulting output signal of the frequency divider is at 3.89 MHz, corresponding to the DCO frequency of 3.98 GHz, which is close enough to the ideal carrier frequency.

6.4.9 Clock Reference

The implemented FM-UWB transceiver does not contain an oscillator that would provide a frequency reference for other circuits (LO calibration,

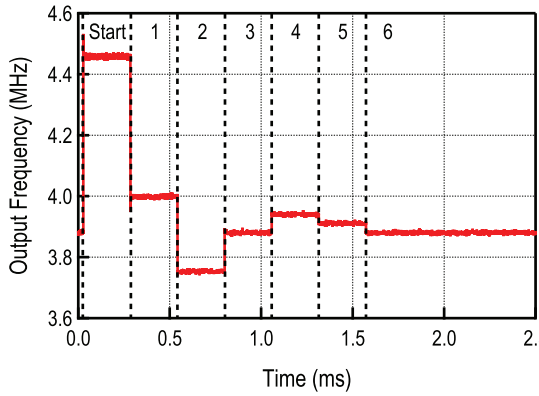


Figure 6.33 Example measured SAR FLL calibration cycle.

N-path filter, FSK demodulator etc.). Instead, the clock signal is generated externally using a signal generator, allowing to adapt to different modes of operation and test the functionality of the transceiver. Since one of the goals of this work is to show that an FM-UWB transceiver can be implemented without a precise, off-chip quartz resonator, one solution for derivation of all the necessary clock signals will be described here.

A simple RC oscillator could be used as a clock reference, similar to one of the solutions found in [22–25]. State of the art precision of 2500 ppm across the temperature range of interest is sufficient for the FM-UWB transceiver developed here. The FSK demodulator and the clock recovery circuit were designed to compensate for the potential frequency offset. At RF this range translates into ± 10 MHz offset around the carrier frequency of 4 GHz, which is well bellow the targeted range of ± 50 MHz. The RC would simply provide the fixed reference clock signal, different frequencies needed for different circuits would be generated using a simple FLL or a DLL (delay locked loop). The block diagram of the conceptual solution with all the related sub-blocks is shown in Figure 6.34.

For the SC-DDS, a clock frequency of at least 40 MHz is needed to provide a relatively good triangular signal. Higher frequencies should provide a better triangular waveform, but would also result in increased power consumption of this block. At the same time the FLL must be able to provide frequencies from 4 MHz to 8 MHz, as a reference for the N-path filter and the FSK demodulator. Luckily, the same frequency is used by both circuits. For the N-path filter, the clock is divided by 4 in order to generate the four non-overlapping phases at the sub-carrier center frequency. The symbol clock

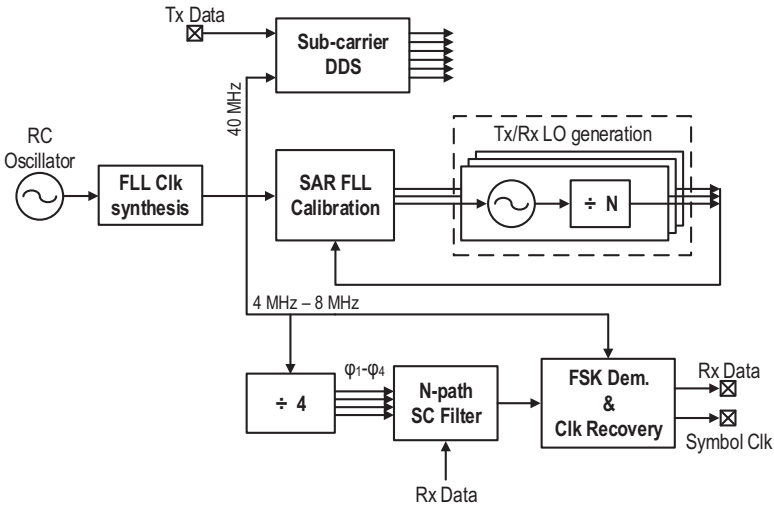


Figure 6.34 Principle of clock generation and distribution.

of approximately 100 kHz is derived from the input clock using a simple counter, and the clock recovery circuit assures that it tracks the symbol rate of the received signal. No particular constraints in terms of input frequency exist for the FLL calibration loop, the two configurable reference values (see Figure 6.32) can always be set such that the DCO frequency is properly calibrated. The proposed clocking scheme can therefore be used to provide a reference to all the circuits in the system, demonstrating one way to implement a fully integrated FM-UWB transceiver.

6.5 Measurement Results

The proposed transceiver was integrated in a standard 65 nm bulk CMOS technology. The SEM die photograph is shown in Figure 6.35. The die size is 2.25 mm by 2.25 mm, and roughly one third of it is the active area of the transceiver (including the decoupling capacitors). The remaining area is used for test circuits and decoupling capacitors. The transceiver layout is dominated by the inductors needed to provide input and output matching. Large inductor area makes routing more difficult and requires longer paths, that consequently add more parasitics at the transceiver IO. It should be noted here that standard TSMC inductors were used for the design. These inductors use only a single metal layer (the low resistance ultra-thick metal), and hence occupy a large area. The layout could be made more compact using smaller,

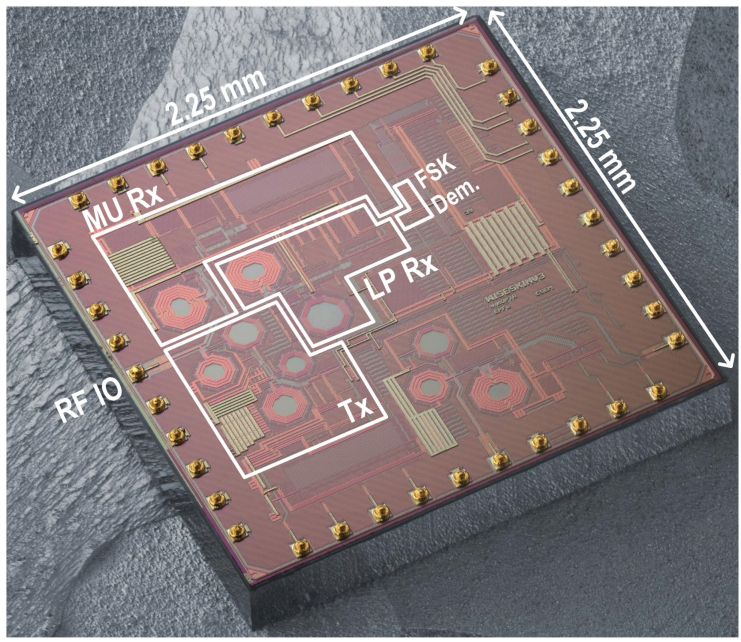


Figure 6.35 SEM die photograph of the transceiver.

more area efficient custom inductors, that would exploit additional available metal layers. The RF IO pad, used by the receivers and the transmitter, is marked in the figure. It is placed between the two ground pads, that are connected to the coplanar waveguide implemented on the PCB. Digital input and output pads, used for test and debug signals, clocks and input and output bits, are located on the side of the chip opposite to the RF IO pad and other sensitive analog signals in order to minimize coupling between strong digital signals and sensitive analog signals. Gold bumps, used for flip-chip bonding of the IC to the PCB, can also be seen in Figure 6.35.

6.5.1 Transmitter Measurements

The first block of the transmitter is the sub-carrier DDS. The static configuration that controls the two sub-carrier frequencies is loaded via the SPI, and the dynamic behavior of the circuit is controlled using the two inputs, the clock and the data input. The SC-DDS controls two current steering DACS, one that drives the DCO, and the other one that drives the test buffer. The output signal from the test buffer is presented in Figure 6.36(a). The shown waveform corresponds to 2.1 MHz sub-carrier signal and 500 MHz wide

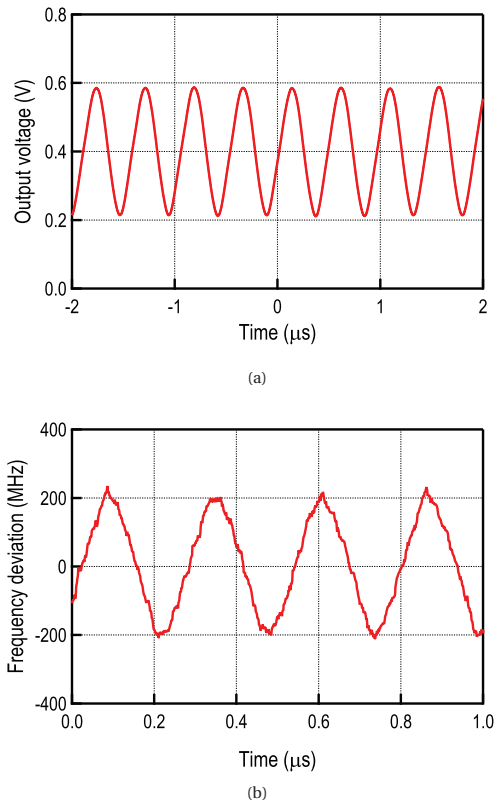


Figure 6.36 Measured sub-carrier DAC output (a) and measured frequency deviation of the transmitted signal (b).

FM-UWB signal. Deviation from the triangular waveform is a result of the limited bandwidth of the buffer. Sub-carrier waveform can also be obtained by directly measuring instantaneous frequency of the transmitted signal. The frequency measurement is done using the Keysight VSA application with the 8 GHz, MSO oscilloscope. The resulting waveform is depicted in Figure 6.36(b). Due to large input bandwidth, the resulting signal is relatively noisy, but still shows some of the properties of the generated SC signal. In this case SC frequency is set to 4 MHz, which is in fact above the targeted SC frequency range. It can be seen in the figure that the output waveform deviates from a triangular close to the peaks. As a result the bandwidth of the output FM-UWB signal will be slightly lower than expected. This is a result of the low oversampling ratio (ratio between the clock frequency and the sub-carrier

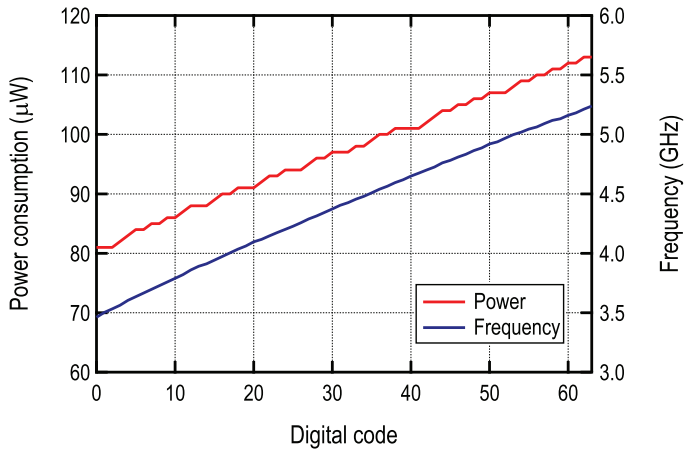


Figure 6.37 Frequency and power consumption of the transmit DCO.

frequency f_{clk}/f_{SC}). In the presented example, the oversampling ratio is 10, for a 40 MHz input clock. According to [2], a relatively good result is obtained for an oversampling ratio of around 20, which will be the case for the desired SC band (1.2 MHz-2.3 MHz).

The measured DCO frequency and power consumption are presented in Figure 6.37. The DCO frequency can be varied from 3.5 GHz to 5.2 GHz and for this range the current consumption varies from 80 μA to 113 μA. This frequency tuning range is achieved using the static DAC that only sets the upper FM-UWB frequency. Dynamic modulation DAC then sinks the current from the static DAC to modulate the carrier frequency. The reported measurement is the consumption of the DCO alone, without the buffer consumption. For the nominal setting, the buffer consumes an additional 71 μA of current. By changing the buffer bias current, the DCO output amplitude can be adjusted, and the consumption can be varied from 48 μA to 94 μA. The input signal amplitude allows to control the output power and current consumption of the PA and PPA, and optimize the transmitter efficiency.

Due to the large bandwidth, FM-UWB signal is inherently robust against carrier offsets. The same property allows it to tolerate relatively high levels of phase noise. It was shown in [3] that phase noise as high as -80 dBc/Hz, at 10 MHz away from the carrier, causes no significant performance degradation in terms of BER. This constraint is quite loose and permits the use of low quality ring oscillators for signal generation. For comparison, consider the Bluetooth standard that imposes a constraint of -102 dBc/Hz

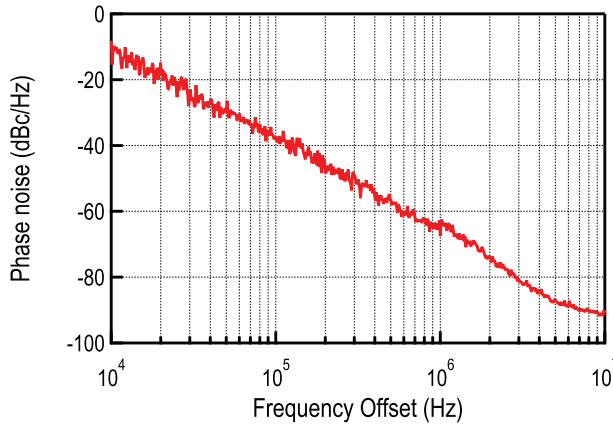
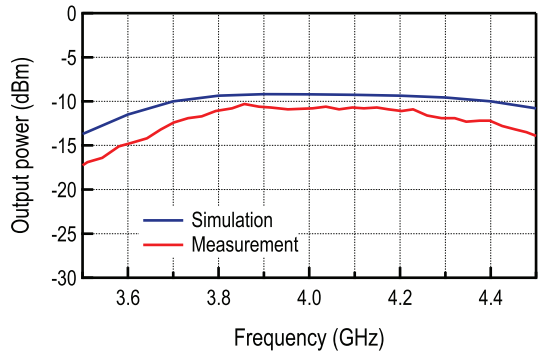


Figure 6.38 Phase noise of the transmit DCO at 4 GHz.

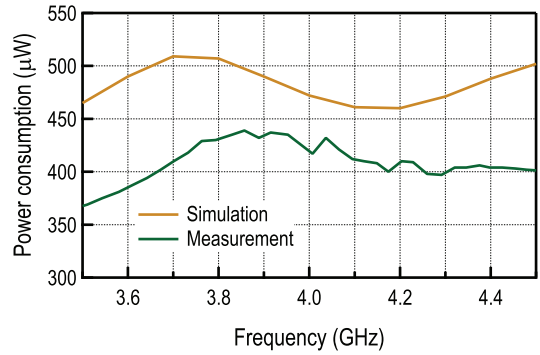
at 2.5 MHz [26], and consequently requires higher power consumption for carrier synthesis. The measured transmit oscillator phase noise, for the oscillation frequency of 4 GHz, is shown in Figure 6.38. At 10 MHz away from the carrier, phase noise level is -98 dBc/Hz, which is considerably lower than the FM-UWB constraint. The phase noise was measured using the signal at the output of the frequency divider. A factor of $20 \log 1024$ was added to the measured phase noise to account for the division ratio of 1024. Noise coming from the dividers will add to the total phase noise at the output; however, due to the already large phase noise of the ring oscillator it should not have a significant impact on the measured value.

The power amplifier and the output matching network were designed to provide good performance over the entire 500 MHz range. The idea is to achieve high average efficiency of the transmitter during wideband signal transmission, and not at a single frequency, which is usually the approach in narrowband systems. Static frequency characteristic of the PA and PPA stack is summarized in Figure 6.39. The measurement is conducted using the DCO as the input signal source, since an external signal cannot be used. For this measurement the DCO is configured to produce a carrier signal at a single frequency. Due to high phase noise and unstable frequency of the ring oscillator, the result is likely worse than it would have been if a clean carrier signal were used.

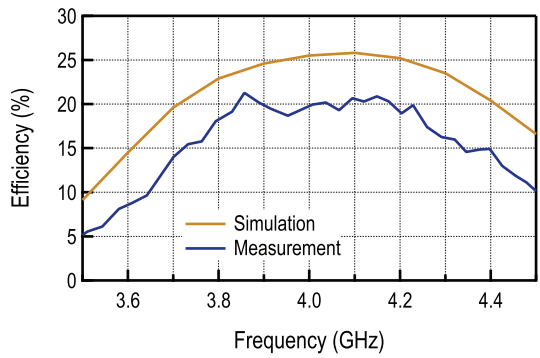
The measured output power of the transmitter is shown in Figure 6.39(a). Compared to simulations, the level is approximately 2 dB lower, with a somewhat smaller bandwidth. The discrepancy between the simulation and



(a)



(b)



(c)

Figure 6.39 Measured power amplifier output power (a), consumption (b) and efficiency (c) including the preamplifier.

measurement is likely caused by the effects that were not taken into account in the simulation. A simplified model of the output pad and the interface toward the PCB were used, more accurate results would have been obtained by using a full 3D electromagnetic simulation. Nevertheless, the error remains within the expected limits of a few decibels. Fortunately, the impedance of the matching network also affects the power consumption. The fact that it slightly differs from the simulated values also results in decreased measured power consumption compared to the simulated one, as shown in Figure 6.39(b). Lower output power, combined with lower power consumption, finally result in efficiency around 6% lower than expected in simulations. As shown in Figure 6.39(c) peak measured efficiency of the output stage (not including the DCO and the buffers) equals 21.3%. In the largest part of the band efficiency stays around 20%, and slowly drops close to the edges of the band, resulting in an average efficiency of around 18%. The measured output power and efficiency of the implemented power amplifier are in line with the state of the art and exhibit similar performance as other implementations targeting low output power levels.

The spectrum of the transmitted signal is presented in Figure 6.40. The shown spectrum is below the limit defined by the FCC spectral mask. Outdoor spectral mask is shown in this case, the only difference between the outdoor and the indoor mask being the attenuation outside the defined UWB band, which is more stringent for the outdoor mask. The transmit signal also satisfies the defined emission level between 0.96 GHz and 1.61 GHz, where maximum level set to −75 dBm/MHz (not shown in Figure 6.40).

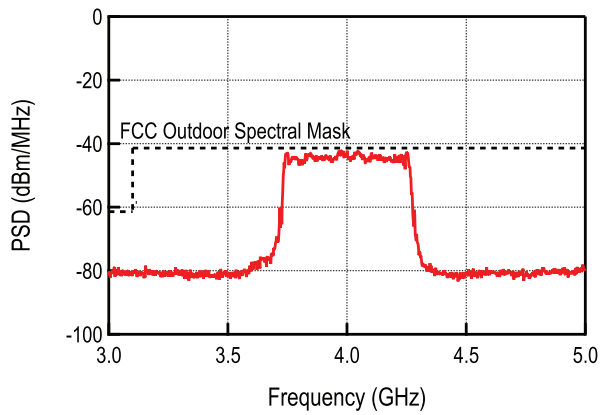


Figure 6.40 Transmitted FM-UWB signal spectrum.

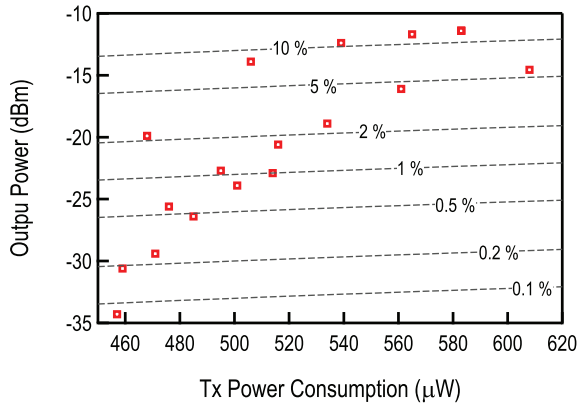


Figure 6.41 Transmit power vs. transmitter power consumption.

Figure 6.41 shows different output power levels and average transmitter power consumption, achievable using different transmitter configurations. Constant efficiency lines are provided to show the achievable efficiency at a given output power. In this case, the whole transmitter is taken into account including the DCO, buffers and SC-DDS (not just the PA and PPA). The shown output power levels are measured as integrated power across the transmit band during a single sub-carrier transmission. The output power level can be varied from -11.3 dBm down to -35 dBm, in steps that are smaller than 3 dB. This is done via the control of the DCO buffer strength (or equivalently PPA input signal amplitude), the PPA bias current and the matching network. The control of the output power can then be implemented using a look-up table in software. The ability to adjust the output power is useful for multi-user communication. For example, if the two transmitting nodes are at different distances from the receiving node, the power levels of the two signals will be different. In order to equalize power levels at the receiver, the closer transmitter can adjust its output power to avoid desensitizing the receiver.

Measured input S_{11} parameter is shown in Figure 6.42. The measurement is done using the die bonded to the PCB, with a 1 cm long coplanar waveguide between the RF IO pad and the horizontal SMA connector. The lower values compared to the simulations are likely related to the PCB, since the connector and the transmission line were not taken into account. On the receiver side, the additional losses coming from the PCB actually improve the reflection coefficient, that is below -10 dB from 3.6 GHz to 4.75 GHz.

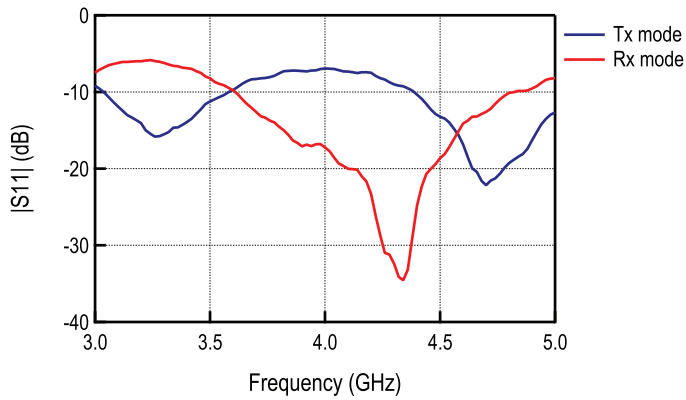


Figure 6.42 Measured S_{11} parameter in transmit and receive mode.

Table 6.1 Transmitter power consumption breakdown

Block	Current Cons. (μA)	Relative Cons. (%)
PA+PPA	402	69.9
DCO	91	15.8
DCO Buffer	71	12.4
SC DDS	11	1.9
Total	575	100

The power consumption breakdown of the transmitter is given in Table 6.1, for the transmitted power of -11.4 dBm. Almost 70% of the power is consumed by the output stage (PPA and PA). In order to improve the efficiency of the transmitter, this part should be carefully optimized in the future. The SC DDS consumption is practically negligible compared to other blocks, and so its implementation will have little impact on the overall performance. The DCO together with the buffers consume slightly less than 30%, thanks to the fact that there is no continuous time PLL or FLL controlling the output frequency.

6.5.2 Receiver Measurements

The two receivers are mainly characterized in terms of BER and sensitivity under different conditions. Unfortunately, there is no way to access different internal points of the receiver and characterize each block separately. Addition of buffers that would allow this would result in increased capacitance in the corresponding nodes, which would consequently increase the receiver

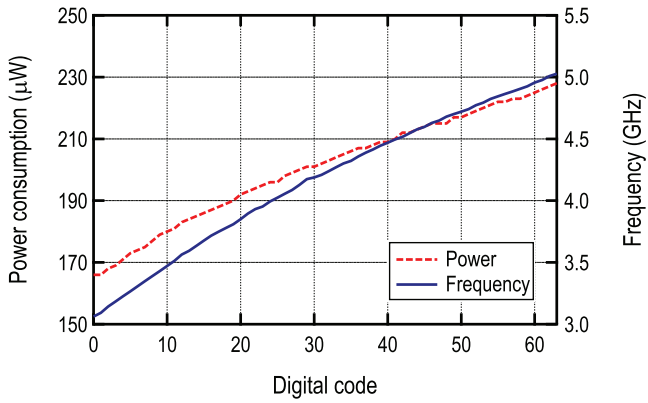


Figure 6.43 Measured frequency and power consumption of the MU Rx DCO.

power consumption. The buffers and test outputs are therefore added only at lower frequencies where such capacitive load causes no significant problems.

The DCOs of the two receivers are the most important blocks in the chain, since without downconversion it would be impossible to perform demodulation. Just like with the transmitter DCO, the frequency dividers are added to provide information about the DCO frequency and to close the FLL calibration loop. Unlike the transmitter DCO, linearity of the frequency characteristic is not needed on the receiver side. What is important is its monotonicity, that ensures proper operation of the SAR FLL loop. The frequency and power consumption of each DCO are measured using the frequency dividers and a digital output buffer. The result for the MU receiver is shown in Figure 6.43. The provided result also includes the four DCO buffers for quadrature LO signals. The oscillator frequency ranges from 3 GHz to 5 GHz, while power consumption changes from 166 μW to 228 μW. The resulting frequency resolution changes from 35 MHz to 20 MHz as the oscillation frequency increases. The same measurement for the LP receiver is given in Figure 6.44. Again, measured power consumption includes the buffer, or in this case the frequency trippler, since it reuses the current from the oscillator. In this case, the output frequency takes values from 3.6 GHz to 5.25 GHz, while it consumes between 51 μW and 77 μW. Due to nonlinear behavior of the oscillator, the frequency step reduces from around 30 MHz at the lower end, to 20 MHz at the high end.

Another block that can be measured standalone is the N-path filter. Figure 6.45 shows the voltage gain characteristic of the filter. Used input clock frequency is 5 MHz, which results in the filter center frequency of

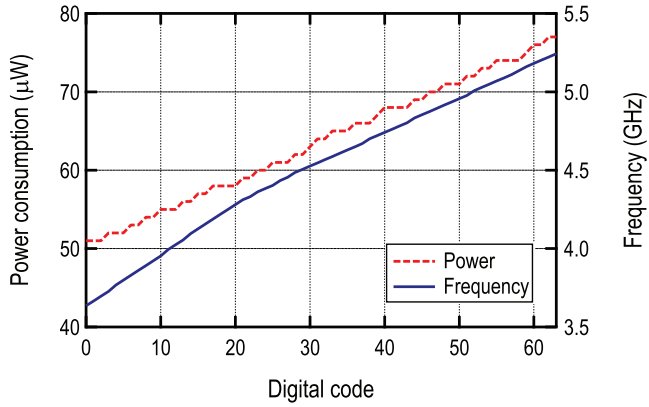


Figure 6.44 Measured frequency and power consumption of the LP Rx DCO.

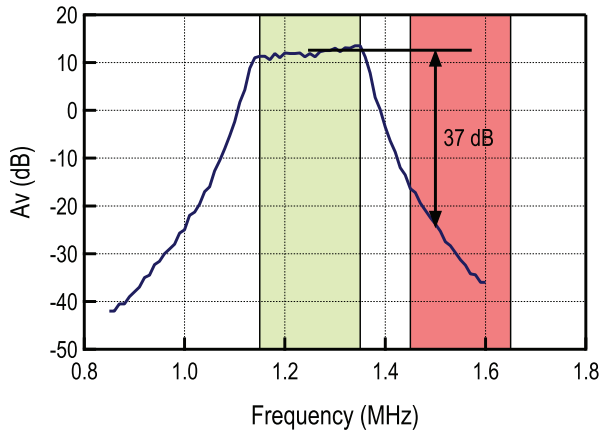


Figure 6.45 N-path filter measured characteristic for center frequency of 1.25 MHz.

1.25 MHz. For the given configuration, the filter provides 200 kHz of bandwidth, and attenuation of 37 dB at the frequency of the adjacent sub-carrier, which is 250 kHz away from the filter center frequency. As expected, the characteristic in the pass-band is not entirely flat. A small inclination appears as a result of parasitic capacitances in the layout, however, for this particular case the performance should not be affected. The purpose of the N-path filter is to remove the interfering sub-carrier channels. As a demonstration, the spectrum before and after the filter is shown in Figure 6.46. Signal spectrum after the wideband FM demodulator is shown in top part of the figure. Four FM-UWB signals of equal power are present at the receiver input. After demodulation,

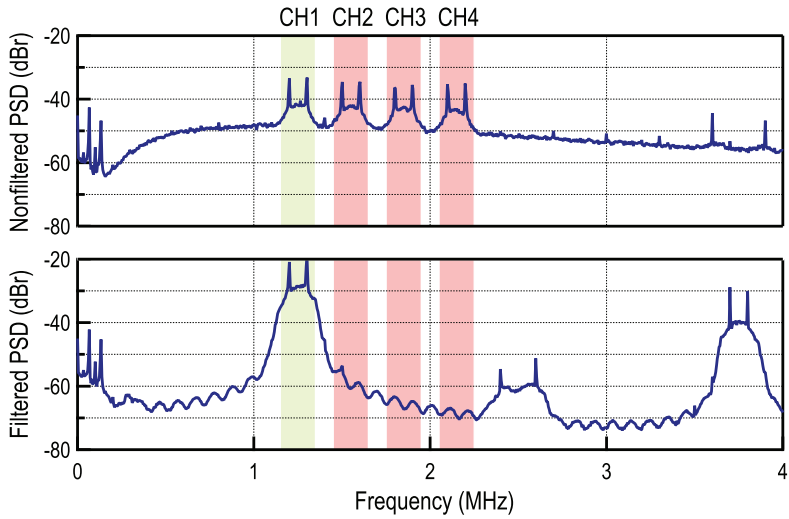


Figure 6.46 Demodulated signal spectrum before and after N-path filter.

four SC channels can be distinguished in the spectrum before filtering. After passing through the filter only channel 1 remains (bottom). Component at 3.75 MHz is a consequence of the sampled nature of the system. With the clock frequency of 1.25 MHz and 4 phases, the equivalent sample rate will be 5 MHz. Attenuated copy of the signal spectrum therefore appears at the frequency $(N-1)f_{clk}$, where n is a number of phases, which is 3.75 MHz. Another visible component is the second harmonic of the SC channel at 2.5 MHz. This component is the combination of the output buffer non-linearity, and mismatch of the N-path filter. Ideally, second harmonic should be completely suppressed by the differential architecture of the N-path filter, however, in practice the amount of attenuation will be limited by matching.

Power consumption breakdown for the MU receiver is given in Table 6.2. As expected the highest amount of power is consumed by the high frequency blocks, the active mixer and the DCO, that together consume around 60% of the entire receiver consumption. The dominant consumer still remains the DCO, with buffers included, that consumes 194 μW. Among the low frequency blocks, notable amount of power is used for the N-path filter that provides sharp band-pass filtering. An overhead necessary to provide the multi-user capability. Finally, the total consumption of the MU receiver is 550 μW. This is more than the receiver presented in the previous section, mainly due to the fact that the baseband processing is now placed on chip.

Table 6.2 MU receiver power consumption breakdown

Block	Current Cons. (μA)	Relative Cons. (%)
LNA/Mixer	153	27.8
DCO	79	14.4
DCO Buffer	115	20.9
IFA	113	20.5
FM Demodulator	13	2.4
Channel filter	43	7.8
LFA	6	1.1
FSK Demodulator	8	1.5
Bias	20	3.6
Total	550	100

Table 6.3 LP receiver power consumption breakdown

Block	Current Cons. (μA)	Relative Cons. (%)
LNA/Mixer	103	38.6
DCO	53	19.9
IFA	46	17.2
FM Demodulator	23	8.6
LFA	11	4.1
FSK Demodulator	14	5.2
Bias	17	6.4
Total	267	100

Power consumption breakdown for the LP receiver is given in Table 6.3. The strategy with power reduction is to reduce power of some of the main consumers from the MU receiver. First, the DCO, that is now single-ended, consumes slightly more than one quarter of the MU DCO consumption, that is 53 μW. One downside of the LP oscillator is the lower output amplitude that will affect the sensitivity. The active mixer, consumes a comparable amount of power, since the architecture is the same, with the only difference that a single differential signal is used at the output (there are no I and Q branches). A second significant power saving is coming from the IF amplifier. Since there is no need for two branches, in the LP receiver the consumption is practically halved compared to the MU receiver case. The IFA consumes 46 μW instead of 113 μW in the MU receiver. The total power consumption adds up to 267 μW for the whole LP receiver chain.

The measurement setup used for the BER measurements is shown in Figure 6.47. The transmit bits and input vectors for signal generators are

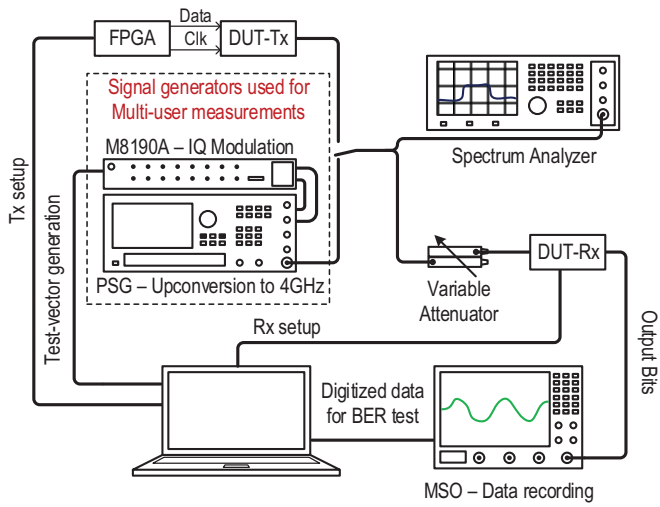


Figure 6.47 Test setup used for transceiver characterization.

created using Matlab. A configured FPGA then provides clock and data inputs for the transmitter. The spectrum analyzer is used to verify that the proper signal is generated by the transmitter and to measure the signal level at the receiver input. Multi-user measurements are still done using the signal generators. This simplifies the setup and allows to precisely control the relative power levels of different FM-UWB signals. The M8190A AWG provides the quadrature baseband signals, which are then up-converted by the PSG. The MSO oscilloscope is used to capture data at the receiver output.

All the BER curves are measured in two ways, first using the offline data post processing, and then using the on-chip FSK demodulator. This allows to measure the loss of the on-chip FSK demodulator compared to the ideal demodulator implemented in software. For the offline BER measurement, the MSO acts as a 20 MS/s, 10 bit ADC that captures analog data after the wideband FM demodulator. This data is then processed using software. First, the desired channel is filtered using an FIR band-pass filter to remove any undesired adjacent sub-channels. Then it is passed through a correlator, that is an optimal detector for the orthogonal FSK modulation used. The output bits are then compared to the generated test vector. In the second measurement, that uses the on-chip FSK demodulator, digital outputs are available, logic analyzer is used to sample data on a rising edge of the recovered clock. It is worth mentioning that the second measurement takes significantly less

time (and memory) since the number of samples is significantly lower and corresponds to the number of bits. In the first case 200 samples are captured per received bit in order to perform the demodulation in software. This corresponds to a sampling frequency roughly 10 times higher than the sub-carrier frequency.

The BER curves for the MU receiver and the single user case are presented in Figure 6.48. The curves for both external (software) and internal demodulator are shown. In the case of the external demodulator the sensitivity is −69 dBm. The result is similar to the previous receiver implementation, with some losses due to a more complex input matching network. The internal demodulator adds 1 dB loss compared to the ideal software demodulator, resulting in a receiver sensitivity of −68 dBm. Accounting for approximately 2 dB loss due to a non-ideal LO, and 1 dB loss due to a non-ideal FSK demodulator, this is roughly 7 dB worse than the theoretical result.

The BER curves for the LP receiver in the single user case are presented in Figure 6.49. Just like in the above case, both curves, for the external and internal demodulator, are shown. In the case of the external demodulator the sensitivity is −58 dBm. Accounting for the theoretical 6 dB difference in sensitivities between the two receivers, and higher noise figure of the LP receiver, the 11 dB degradation in sensitivity is expected. Compared to the theoretical sensitivity, same 7 dB degradation is observed as in the case of the MU receiver. This is the price to pay for lower power consumption of the LP receiver. Again, the simple, low power internal demodulator adds some loss,

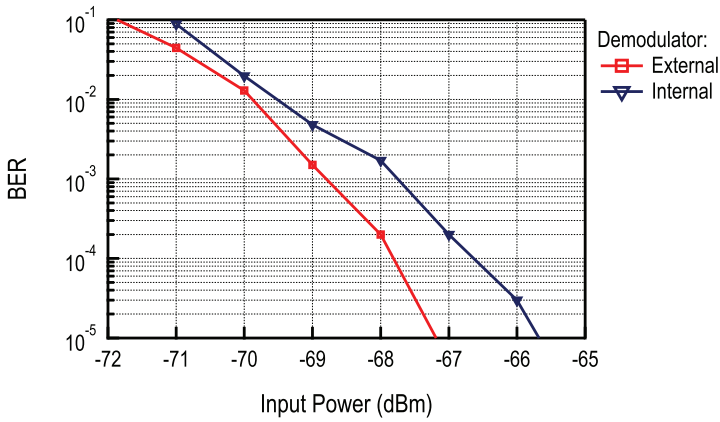


Figure 6.48 Single user BER of the MU Rx with internal and external demodulator at 100 kb/s.

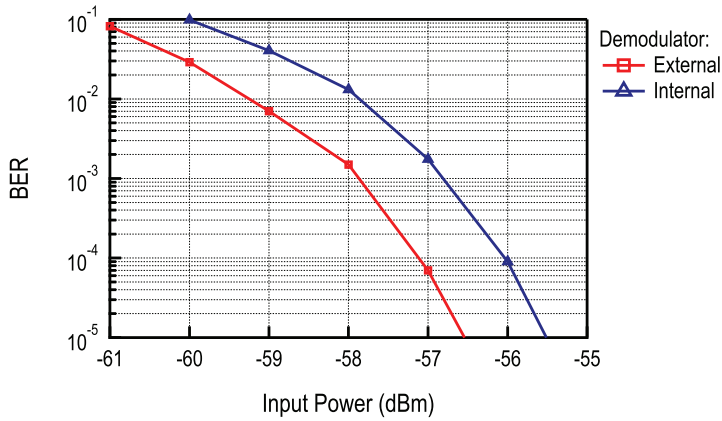


Figure 6.49 Single user BER of the LP Rx with internal and external demodulator at 100 kb/s.

resulting in −57 dBm sensitivity of the LP receiver. Although sensitivity is relatively low compared to other FM-UWB receivers, it is still enough for short range communication in a WBAN, and the implemented receiver consumes the lowest amount of power among all the implementations reported in literature.

A photo of the measurement setup is shown in Figure 6.50. Two boards can be seen in the figure, one is used as a transmitter and the other one as a receiver. The signal level on the receiver side is controlled using a configurable attenuator. Spectrum analyzer, showing the FM-UWB signal spectrum, is used to verify the proper operation of the transmitter and can be seen in the right part of the figure. In this case, the oscilloscope is used to compare the transmitted and the received bits. The recording from the screen is shown clearly on the graph. Aside from the input and output data, the graph also shows the recovered clock used for sampling the output data. A delay of approximately 20 μs can be seen between the transmit and receive bit stream. In the shown example there are no errors present at the output.

The sensitivity of the receiver degrades in the presence of interferers. The behavior of the receiver is evaluated in the presence of a narrowband interferer inside and outside of the used FM-UWB band. The interferer is generated using a separate signal generator and the outputs are summed together using a power combiner. For the in-band interferer, a frequency of 4.1 GHz was chosen as the worst case. Placing the interferer close to the signal center frequency would attenuate it due to the high-pass characteristic of the IF amplifier, and placing it closer to edge of the band would again

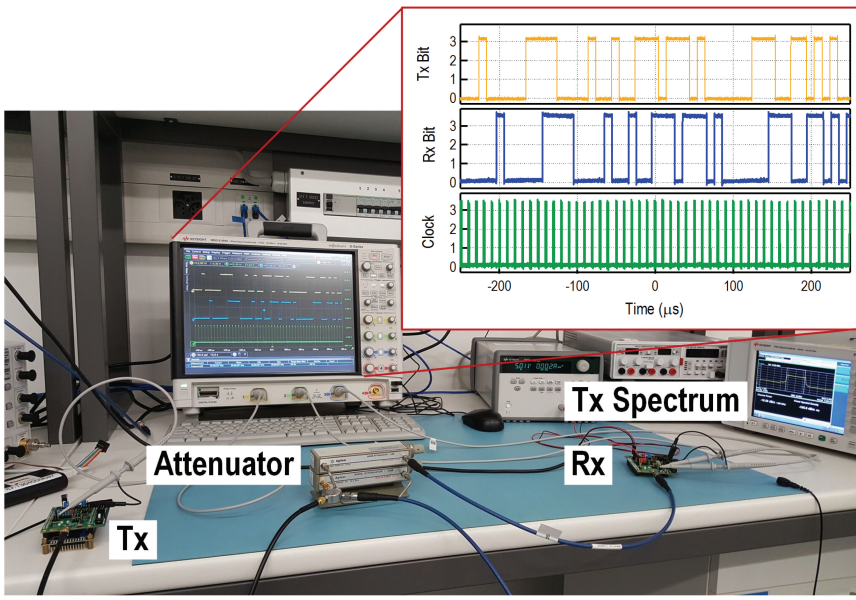


Figure 6.50 Measurement setup and comparison of transmit and received bits.

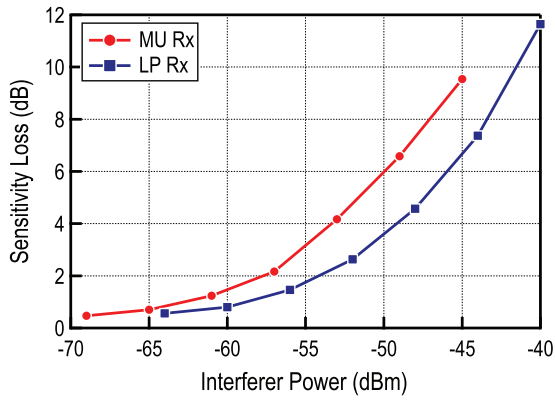


Figure 6.51 Sensitivity degradation due to the presence of an in-band interferer.

result in slightly lower IF gain due to the IFA low-pass behavior. The same frequency was used for both MU and LP receiver. The sensitivity degradation with the increase of interferer power is shown in Figure 6.51. Assuming 3 dB sensitivity degradation is acceptable, the MU and LP receiver can tolerate up to −55 dBm and −52 dBm strong interferers respectively.

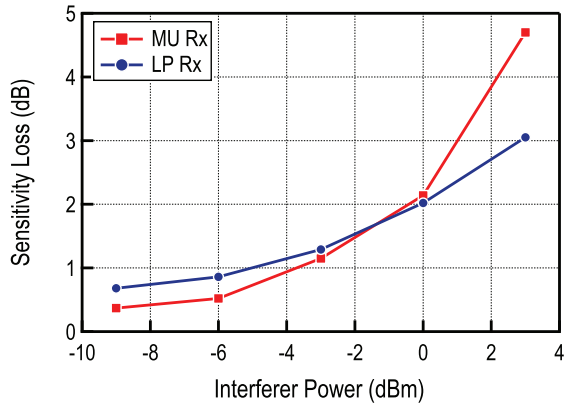


Figure 6.52 Sensitivity degradation due to the presence of an out of band interferer at 2.4 GHz.

For the out of band interferer case, the frequency of 2.4 GHz was chosen. The reason is that the 2.4 GHz ISM band (industrial, scientific and medical) is commonly used by different short range BAN devices. The sensitivity degradation in the presence of an out of band interferer is shown in Figure 6.52. Assuming again 3 dB sensitivity loss is acceptable, the MU receiver can tolerate 1 dBm interferer and the LP receiver can tolerate a 3 dBm interferer at 2.4 GHz. This is much higher than any other implementation and is due to the sharp filtering characteristic of the IF amplifier, that acts as a 6th order low pass filter. In most other implementations the interferer is only attenuated by the 2nd order LNA input matching network. This means that the proposed FM-UWB receivers can operate reliably next to any other device using the ISM band (such as a BLE radio for example).

As discussed previously, FM-UWB is inherently robust against frequency offsets thanks to its large bandwidth. This is clear when it comes to tolerance to LO signal offset, however the property also applies to other parts of the system. After the wideband FM demodulation, the sub-carrier channels are located between 1.2 MHz and 2.3 MHz. An offset of 1000 ppm translates into a maximum sub-carrier offset of 2.3 kHz, which would still not prevent correct FSK demodulation. For comparison, assume the same 1000 ppm offset is present in a Bluetooth transmitter that operates in the 2.4 GHz band. This would translate into an offset of 2.4 MHz, which is larger than a Bluetooth channel bandwidth. The example illustrates why an FM-UWB system has an advantage compared to typical narrowband systems. In fact, the FM-UWB receiver can tolerate a frequency offset much

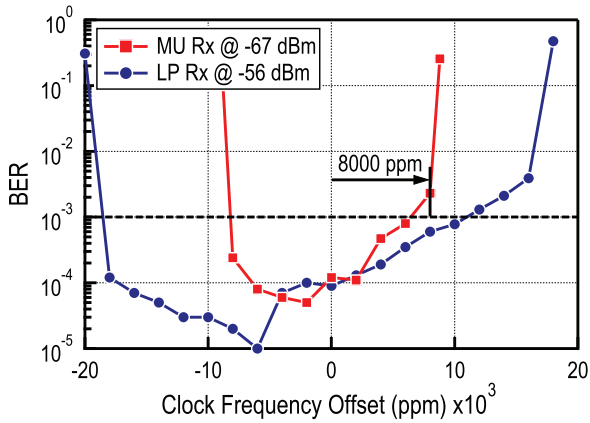


Figure 6.53 BER for a fixed input signal level with varying reference clock frequency.

larger than 1000 ppm. Figure 6.53 shows the BER of the two receivers as a function of the receiver reference clock offset. The curves were measured at 1 dB below the sensitivity level, that is −67 dBm for the MU receiver and −56 dBm for the LP receiver. They show the amount of offset that can be tolerated before the sensitivity increases by 1 dB. Measurement was done with the fixed transmitter frequency reference and variable reference on the receiver side. Looking at the curves, two parts can be distinguished. The first is at relatively small offsets, where there is only a minor degradation in terms of BER. Then, it can be noticed that after offset increases beyond a certain point there is a sharp increase in BER. This is the region where clock recovery fails, and errors occur in sampling the decoded bits, which results in BER around 0.5. Interestingly, the LP receiver shows less degradation at higher offsets. The reason is that the sub-carrier frequency of the demodulated signal doubles after demodulation by the LP receiver. As a consequence, the frequency deviation will be doubled and the FSK demodulator will be able to operate more reliably at higher offsets. Both receivers are still able to perform reliable demodulation at offsets below 8000 ppm. This value is above the reported frequency deviation in state-of-the-art on-chip reference oscillators. Therefore, the presented measurements clearly show that it is feasible to make a fully integrated FM-UWB transceiver, without external resonators for a reference clock.

The main advantage of the proposed MU receiver is the ability to distinguish multiple FM-UWB signals at the receiver input, provided that the

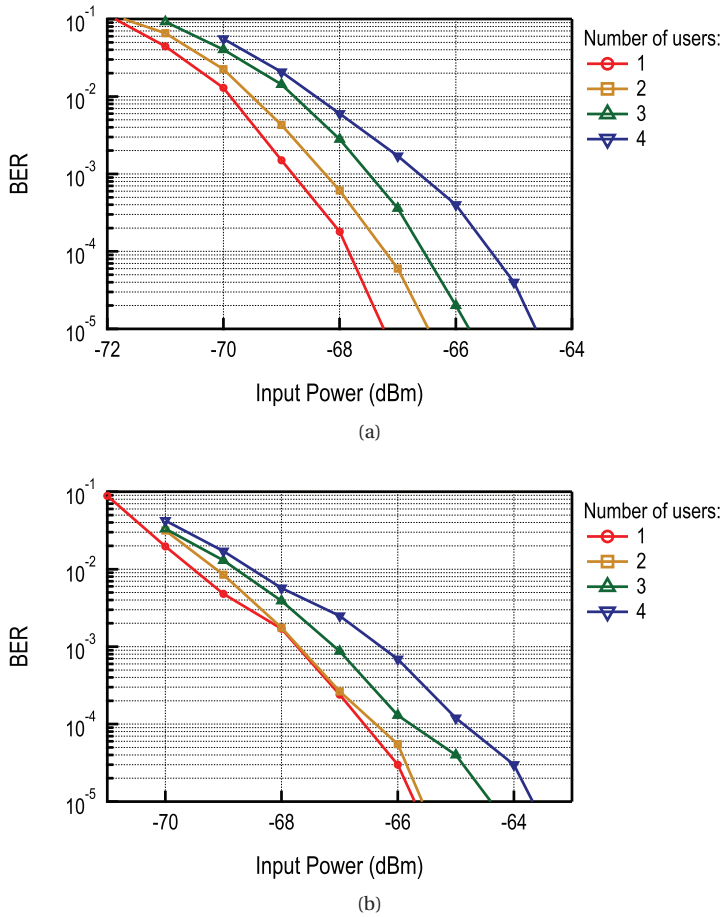
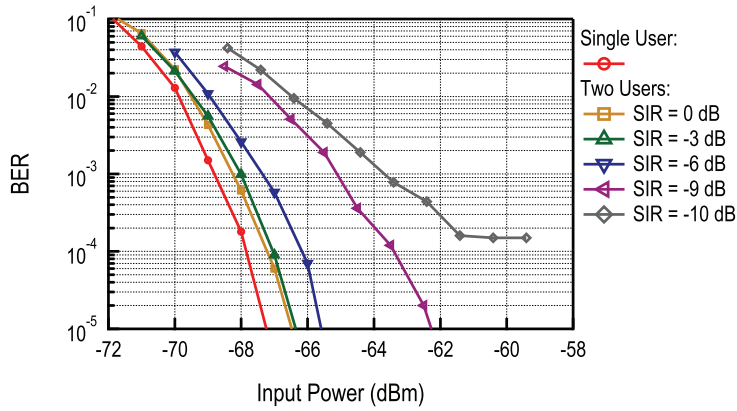
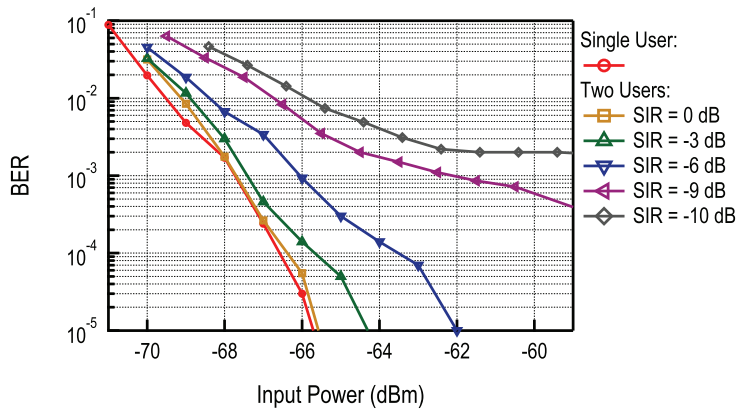


Figure 6.54 Measured BER curves for multiple FM-UWB users of same power level, demodulated with external (a) and internal (b) demodulator.

sub-carrier frequencies are different. In the first scenario, multiple FM-UWB signals of equal power are present at the input. The measurement with the external demodulator is shown in Figure 6.54(a), and the measurement with the internal FSK demodulator is shown in Figure 6.54(b). The curves behave in a similar manner in both cases. As the number of users increases so does the inter-user interference and, as a result, the sensitivity degrades. In the case with 4 users a degradation of roughly 2 dB can be observed from the graph. As long as the power levels at the receiver input remain approximately equal, there will be no significant performance degradation.



(a)



(b)

Figure 6.55 Measured BER curves for two FM-UWB users of different power levels, demodulated with external (a) and internal (b) demodulator.

If several transmitting nodes are located at different distances from the receiving node, they can adjust the their power levels so that the power at the receiver remains the same, and avoid the excessive sensitivity loss. This is the main reason why a transmitter that can adjust output power is useful for a HD-WSN.

A scenario with 2 users and a variable difference in power levels is shown in Figure 6.55. Again, the inter-user interference increases with the increase in interferer power, and the resulting sensitivity degrades. With a sufficiently strong interferer at the input, the achievable SNIR after the first

FM demodulation becomes limited by the interference, and the resulting BER curve flattens. The difference between the external and internal demodulation is clearly visible in Figures 6.55(a) and 6.55(b). In both cases 10 dB stronger interferer results in a floor for the achievable BER. Since the external demodulator needs a 1 dB lower SNIR for the same performance, the BER curve flattens below $2 \cdot 10^{-4}$. In the case of the internal demodulator, the curve flattens at $2 \cdot 10^{-3}$, and the desired sensitivity level remains unreachable. With the internal demodulator the receiver is capable of demodulating data if the difference of input levels is 9 dB or smaller. The limit is due to a combination of interference coming from the leakage of adjacent FSK sub-channels and cross modulation products between the two users in the process of the first FM demodulation.

6.6 Summary

A fully-integrated FM-UWB transceiver has been presented in this chapter. A single RF IO port is used, with an on-chip matching network, which eliminates the need for external passive components or switches. Two receivers provide two different modes of operation. The low power mode reduces the power consumption to 267 μW, but only allows a single FM-UWB channel. To improve sensitivity and allow SC-FDMA, a MU receiver is used, that allows up to 4 FM-UWB transmitters to operate at the same time and in the same RF band. Inherent robustness against narrowband interferers, combined with sharp IF filtering, result in good in-band and out of band interferer rejection. This capability could allow to power the transceiver wirelessly using a 2.4 GHz narrowband signal. Finally, the transceiver is robust against reference clock offsets of up to 8000 ppm, effectively eliminating the need for an off-chip reference. Performance summary and comparison with the state of the art is given in Table 6.4.

The architecture of the implemented transmitter is very similar to the one from [3]. The solution from [3] uses a three stage DCO that generates one third of the carrier frequency. The three phases are combined using a frequency trippler that generates the FM-UWB signal. The trippler reuses the current of the power amplifier in order to minimize power consumption. One of the downsides of that approach is that the signal at one third of the frequency appears at the output together with its harmonics, which might violate the spectral mask. The second issue is that the trippler output power cannot be precisely controlled, which is a useful feature when a large number of nodes operate in a small area. In the proposed implementation this problem

Table 6.4 Comparison with the state-of-the-art transceivers

Parameter	[27][(1, 2)]	[28]	[3]	This Work	
				LP	MU
Modulation	FM-UWB	Chirp-UWB	FM-UWB	FM-UWB	
Frequency	7.5 GHz	8 GHz	4 GHz	4 GHz	
Frequency deviation	25 kHz	–	250 kHz	50 kHz	
Receiver Cons.	9.1 mW	4/0.6 mW[(3)]	580 μW	267 μW	550 μW
Data Rate	50 kb/s	1 Mb/s	100 kb/s	100 kb/s	
FSK Sub-channels	2	No	No	No	4
SIR UWB	–	–	–	–	–9 dB
Matching Network	Ext.	Ext.	Ext.	Internal	
NB Interferer Power (in band)	−55 dBm	–	−52 dB[(4)]	−52 dBm	−55 dBm
NB Interferer Power (@ 2.4 GHz)	−38 dBm @ 6 GHz	–	−38 dB[(4)]	3 dBm	1 dBm
Ref. Clock Offset	–	–	–	8000 ppm	
Sensitivity	−88 dBm	−76 dBm	−80.5 dBm	−57 dBm	−68 dBm
Transmitter Cons.	–	2.8/0.42 mW[(3)]	630 μW	583 μW	
Output Power	–	–	−12.8 dBm	−11.4 dBm	
Technology	0.25 μm BiCMOS	65 nm	90 nm	65 nm	

[(1)] Off-chip sub-carrier FSK demodulation [(2)] Receiver only [(3)] Without/with duty-cycling [(4)] −70 dBm input signal power.

is solved by replacing the trippler with a class AB amplifier that drives the main PA. The output power can be regulated using the amplifier bias point, that also sets the bias of the main PA. In addition, the configurable buffer current, and matching network provide additional knobs for output power control, allowing steps smaller than 3 dB. The DCO directly produces the signal at 4 GHz, avoiding the problem with the spectral mask violation. The DCO together with buffers consumes slightly more than the DCO from [3], but this is compensated with a more efficient PA design, so that the overall transmitter consumption still improves.

The proposed receiver targets short range communication in a HD-WSN. Therefore, sensitivity constraint is not very stringent and emphasis is on reducing power and providing means for multi-user communication. The receiver from [3] achieves very good sensitivity and low power consumption,

but the demodulator characteristic is highly non-linear and it cannot support multiple sub-carrier channels. In addition it uses a frequency deviation of 250 kHz (or equivalently 500 kHz separation between the two sub-carrier frequencies), which allows for a simpler FSK demodulator implementation. In this work, frequency deviation is reduced to 50 kHz in order to allow for multiple sub-carrier channels. A different demodulator implementation is necessary in order to demodulate an FSK signal with a modulation index of 1, which will consume slightly more power. Potential for multi-user communication with FM-UWB has been demonstrated before, for example, two different sub-carrier channels could be seen at the demodulator output from [27]. However, this implementation was only providing the first FM-UWB demodulation. The proposed receiver is the only fully integrated solution that provides support for multi-user communication. In addition, it also incorporates a clock recovery circuit that demonstrates the feasibility to integrate the full transceiver with no need for an off-chip crystal reference.

In this case there was no need for higher data rates, although it could be a topic of future research. Increasing data rate of the FM-UWB receiver would mainly require modifications in baseband, and so the overhead in terms of power consumption should remain very low. This should lead to a more efficient implementation, that could achieve even lower energy per bit. Multi-user communication could be explored further, combining either larger number of lower data rate channels, or fewer channels that provide higher data rates, depending on the needs of the specific application. Finally, there could be more room for improvements at the modulation level. The Chirp-UWB concept, that is positioned somewhere between the IR and FM UWB, provides higher data rates, without a significant increase in complexity, and symbol level duty cycling of the receiver provides very low power consumption. Similar modifications could be a topic of future research and could lead to different performance trade-offs.

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