
Contents

Preface	xiii
Acknowledgements	xv
List of Contributors	xvii
List of Figures	xix
List of Tables	xxxvii
List of Abbreviations	xxxix
1 Space Radiation Effects in Electronics	1
<i>Luigi Dilillo, Alexandre Bosser, Arto Javanainen and Ari Virtanen</i>	
1.1 Space Radiation Environment	2
1.1.1 The Sun	2
1.1.2 The Sunspot Cycle	2
1.1.3 Solar Flares and Coronal Mass Ejections	3
1.1.4 Trapped Particles – Van Allen Belts	4
1.1.5 South Atlantic Anomaly	5
1.1.6 Galactic Cosmic Rays	6
1.1.7 Space Weather	7
1.1.8 Atmospheric and Ground-Level Radiation Environments	8
1.1.9 Cosmic Rays	9
1.1.10 Radionuclides in the Soil	10
1.1.11 Thermal Neutrons	11
1.1.12 Artificial Radiation Sources	12
1.2 Radiation Effect in Materials and Devices	12
1.2.1 Energetic Charged Particles and Matter	12

1.2.2	Stopping Nomenclature	14
1.2.3	General Theory for Electronic Stopping	14
1.2.4	Stopping Theories and Semi-Empirical Models	15
1.2.5	Nuclear Stopping Force	16
1.2.6	Ion-induced Nuclear Reactions	17
1.3	Radiation Effects in Semiconductors	18
1.3.1	Generation of Electron–Hole Pairs	18
1.3.2	Nuclear Reactions	19
1.3.3	Linear Energy Transfer vs. Electronic Stopping Force	21
1.3.4	Spatially Restricted LET	22
1.3.5	Energy Loss Straggling	23
1.3.6	Applicability of LET	25
1.3.7	Prediction Tools for Stopping Force	26
1.3.8	Cumulative Effect: Total Ionizing Dose and Displacement Damage	28
1.3.9	Single Event Effects	28
1.3.10	Soft Errors	29
1.3.11	Hard Errors	30
1.4	Effect of Radiation on Memory Devices	31
1.4.1	Structure of a Memory	31
1.4.2	Classification and Fault Mechanisms in Memories	35
1.4.3	Memory Accelerated Tests	38
1.4.4	Test Methods	39
1.4.5	Static Mode Testing	40
1.4.6	Dynamic Mode Testing	41
1.5	Radiation Hardness Assurance Testing	43
1.5.1	Beam Requirements	46
1.5.2	TID Tests	47
1.5.3	TNID Tests	48
1.5.4	SEE Tests	48
1.5.5	Sample Preparation	48
1.5.6	TID Tests	48
1.5.7	SEE Tests	49
1.5.8	Radiation Facilities	49
1.5.9	ESA European Component Irradiation Facilities (ECIF)	49
1.5.10	Other Outstanding European Facilities	50
1.5.11	Other Outstanding Facilities in the World	51

1.5.12	Accelerated Test for Memories	51
1.5.13	Memory Test Setup	52
1.5.14	Notes on Test Result Analysis	54
1.6	Conclusion	55
	References	56
2	RHBD Techniques for Memories	65
	<i>Cristiano Calligaro</i>	
2.1	Effect of HEPs on Semiconductor Devices	65
2.2	Cumulative Effect: TID	68
2.3	Single Event Latch-up: SEL	74
2.4	Single Event Upset: SEU	76
2.5	From SET to SEU/SEFI/MBU: When a Disturbance Becomes an Error	79
2.6	Radiation Hardening By Design (RHBD)	83
2.7	RHBD at Architectural Level	87
2.8	RHBD at Circuit Level	91
2.9	RHBD at Layout Level	95
2.10	Conclusion	100
	References	101
3	Rad-hard SRAMs	103
	<i>Cristiano Calligaro</i>	
3.1	SRAM Foundations: Single Port and Multiple Port	103
3.2	Synchronous or Asynchronous?	118
3.3	SRAM Architectures	124
3.4	Embedded SRAMs	132
3.5	SRAMs' Building Blocks... Rad-hard of Course	136
3.5.1	Input Buffers and ATDs	136
3.5.2	DEMUXs	139
3.5.3	Sensing	140
3.6	ECC Foundations: The Hamming Code	143
	References	149
4	One-Time Programmable Memories for Harsh Environments	151
	<i>Umberto Gatti</i>	
4.1	Introduction	151
4.1.1	NVM Technology Overview	152
4.1.2	OTP Application in Harsh Environments	154

4.2	OTP Memories for Standard CMOS Technologies	157
4.2.1	Principle of Operation	158
4.2.2	CMOS OTP Based on Anti-Fuse	161
4.2.3	Characteristics and Limits	166
4.3	Rad-hard CMOS OTP	169
4.3.1	Critical Features	169
4.3.2	State of the Art	174
4.3.3	RHBD Mitigation: Architectures and Layout	176
4.4	Conclusion	186
	References	186

5 Rad-hard Flash Memories 191

Anna Arbat Casas

5.1	Introduction	191
5.1.1	Non-volatile Memories Overview	192
5.1.2	Flash NVM: Principle of Operation	194
5.1.3	Flash NVM Standard Architecture Overview: NOR vs. NAND	195
5.1.3.1	NOR-Flash	195
5.1.3.2	NAND-Flash	197
5.1.3.3	Summary	198
5.2	Radiation-hard Flash Architecture Study	198
5.2.1	Critical Features: Introduction of the Differential Cell Architecture	199
5.2.2	Program – Erase Circuit Analysis	202
5.2.3	Read & Verify Circuit Analysis	207
5.2.4	General Architecture Considerations and Internal Bit Structure	211
5.2.5	Case Study: FP7 SkyFlash Project on Rad-hard Non-Volatile Memories	213
5.3	Side-Circuits	218
5.3.1	Charge Pump Analysis	219
5.3.2	Charge Pump	221
5.3.3	Pad-ring Requirements	222
5.4	Conclusion	223
	References	223

6	Radiation Hardness of Foundry NVM Technologies	227
	<i>Evgeny Pikhay, Cristiano Calligaro and Yakov Roizin</i>	
6.1	Introduction	228
6.2	Physical Phenomena in CMOS Devices Under Irradiation and Their Control	230
6.3	Radiation Hardness of CMOS Logic Memories	234
6.3.1	Single-Poly EEPROMs	234
6.3.2	GOX Anti-Fuses	236
6.3.3	Radioisotope-Powered Memory	238
6.3.4	Silicon Nitride-Based Memories	239
6.4	On the Chip Tools for TID Radiation Effects Control	247
6.4.1	MOS Structures for Monitoring of Radiation-Induced Charges in Dielectrics	248
6.4.2	FG Devices for Monitoring the TID	252
6.4.2.1	Introduction	252
6.4.2.2	C-Sensor operation principle	256
6.4.2.3	Implementation of C-Sensor principle in CMOS platform	258
6.4.2.4	Detecting different types of ionizing radiation using C-Sensor	259
6.5	Conclusion	264
	References	264
7	Rad-hard Resistive Memories	269
	<i>Cristiano Calligaro</i>	
7.1	ReRAM Cell	269
7.2	ReRAM Array	271
7.3	ReRAM Architecture	277
7.4	ReRAM Periphery	281
7.5	Forming, Setting and Resetting a Resistive Memory	292
7.6	Resistive OTPs (ROTPs): The ReRAM Pioneers	302
	References	305
8	Technologies for Rad-hard Resistive Memories	309
	<i>Christian Wenger</i>	
8.1	Non-Volatile Memory Technologies	309
8.1.1	State-of-the-Art NVMs – Flash Memory	311
8.1.2	The Way-out Over Emerging Technologies	312
8.1.3	ReRAM Technology	313

8.2	Reliability Issues of 1T-1R-based HfO ₂ ReRAM Arrays . . .	315
8.2.1	Retention Results on Amorphous and Polycrystalline Arrays	322
8.2.2	Set Evolution	322
8.2.3	Reset Evolution	324
8.2.4	Impact of Temperature on Conduction Mechanisms and Switching Parameters in HfO ₂ -based 1T-1R ReRAM Devices	327
8.3	CMOS Integration of Resistive Memory Cells	330
8.4	Conclusions	337
	References	338
9	New Generation of NVMs Based on Graphene-related Nanomaterials	341
	<i>Paolo Bondavalli</i>	
9.1	Introduction	342
9.2	Graphene-based Non-volatile Memories	343
9.2.1	Graphene and Graphitic Layers	344
9.2.2	Non-volatile Resistive Memories Based on GO and R-GO Oxide Layers	348
9.3	Other Approaches to Achieve Non-volatile Memories Using Graphitic Layers	354
9.3.1	Graphitic-based Non-volatile Memory Using a Transistor Configuration	355
9.3.2	Non-volatile Flash-type Memories Based on Graphene/Multi-layered Graphene	357
9.4	Conclusions	360
	References	361
	Index	369
	About the Editors	373