# 5

# Quadrature Approximate Zero-IF FM-UWB Receiver

## 5.1 Introduction

The previous chapters explained the basics of FM-UWB modulation, discussed the existing state of the art and introduced two new architectures for an FM-UWB receiver. The concept of the proposed approximate zero-IF architecture with quadrature downconversion is brought to life in this chapter. The work is mainly oriented toward exploiting the short communication range, in order to lower power consumption of the receiver, but also to provide means to efficiently communicate as the number of sensor nodes in the network scales up. This is achieved through the use of the sub-carrier FDMA, that allows to distinguish multiple FM-UWB signals sharing the same RF band.

The chapter starts by introducing the top-level architecture of the integrated receiver. The following section deals with the details of circuit design, focusing on the key approaches and techniques used to reduce the power consumption of the most important circuits. Measurements of the implemented receiver are presented in Section 4.3. Beyond the intended data rate of 100 kb/s, the receiver is characterized in additional scenarios (higher speed, M-FSK modulation, multi-channel transmission) showing the true potential of the FM-UWB modulation. Finally, the chapter is concluded with a summary of achieved results and a comparison with similar receivers from the literature.

## 5.2 Receiver Architecture

The aim of this work is to reduce power of the FM-UWB receivers beyond the current state of the art while preserving the demodulator linearity and multi-user communication capability. As the LNA and other blocks operating at RF have been shown to consume the most power in previously implemented

receivers, the strategy here is to first downconvert the signal to baseband, and then perform all the processing at low frequencies. Since power consumption in all of these blocks typically increases with frequency, moving them to baseband should result in significant power savings.

An oscillator, that was not needed in previous FM-UWB receiver implementations, is now necessary to generate the LO signal. Only if the LO can be implemented with a reasonable power budget can the approximate zero-IF architecture lower the overall consumption. Fortunately, ring oscillators in deep sub-micron technology nodes are known to consume very little and can be used here for such LO generation. The downside of using a low power ring oscillator is its high phase-noise, unstable oscillation frequency and high susceptibility to environmental changes. Ring oscillators are almost exclusively used in closed loop systems such as PLLs, where the oscillator is locked to a reference frequency, and all the aforementioned problems disappear. However, a PLL would require frequency dividers and these would add a significant contribution to the receiver power consumption. Instead of implementing a PLL, a free-running oscillator is used for this implementation and owing to the large FM-UWB signal bandwidth, some of the issues, such as phase noise, are circumvented. Frequency dividers are still needed, but they are used as a part of the FLL calibration loop and are turned on only when calibration is necessary. That is mostly to compensate for frequency drift due to temperature or supply voltage variations. Fortunately, since these changes are slow and the calibration is not needed very often, the FLL calibration circuits will not pose a significant overhead to the receiver consumption.

The high-level block diagram of the implemented receiver is shown in Figure 5.1, with the main receiver at the bottom and the test receiver at the top. The two receivers are implemented in order to asses the performance loss due to the on-chip, low power ring oscillator. They are identical in all aspects except for the LO. The main receiver uses the ring oscillator, whereas the test receiver uses an external signal to drive the mixer. Since this is a direct conversion receiver, quadrature LO signals are generally needed to perform correct demodulation. In the main receiver these are generated directly by the ring (multiple stages produce different phases, as will be shown later), while the test receiver uses an RC-CR network to provide quadrature signals, allowing to reduce the number of input pads. The difference in performance between the two receivers will be reported in the measurement section.

As already mentioned, the idea is to reduce power consumption by removing the RF blocks. It can be seen in Figure 5.1 that the LNA is still present, however, in this implementation it is simply a transconductance amplifier

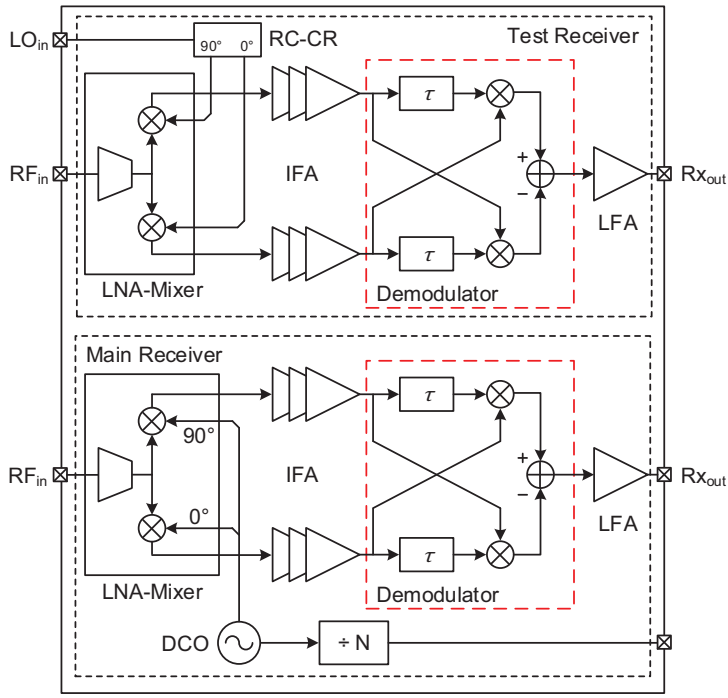



**Figure 5.1** Receiver block diagram.

that converts the input voltage into current that is then downconverted by the mixer. The two can also be regarded as an active mixer with an input matching network. Since this is practically a mixer-first receiver the noise figure will be higher compared to a more standard approach with the LNA in front, but this remains an acceptable price for the achieved power savings. The main gain stages are placed at baseband (here referred to as IF amplifiers), allowing to achieve higher gain at lower power. Since the oscillation frequency of the ring oscillator is not stable, the bandwidth of these amplifiers is increased to account for a $\pm 50$ MHz carrier frequency offset. Instead of 250 MHz that would normally be sufficient to amplify a downconverted 500 MHz wide signal, the bandwidth of IF amplifiers is extended to 300 MHz. The IQ delay line demodulator is a modified version of the demodulator from [1], adjusted for baseband operation, as described in the previous chapter.

The receiver presented here only implements the first FM demodulation. The resulting demodulated sub-carrier signal is buffered and is available at the receiver output. This signal is then converted to digital domain using

an ADC, allowing the further data processing to be conducted off-line. The second FSK demodulation, and all the additional baseband processing (e.g. channel filtering) is implemented in software, allowing to measure BER performance of the receiver. It should be noted that this idealized approach yields a somewhat better performance than otherwise achievable with a low-power hardware implementation, but can nevertheless be used to assess the performance of the integrated blocks. All of the implemented circuits can be controlled through an SPI bus, allowing to tune the bias current, resonance frequency, gain and bandwidth of different blocks and switch them on or off. Details of circuit implementation are given in the following section.

## 5.3 Circuit Implementation

### 5.3.1 RF Frontend

The LNA and the mixer, shown in Figure 5.2, are stacked in order to save power. The circuit can also be seen as an active mixer with the input matching network. An active mixer is chosen for downconversion because unlike a passive mixer, it provides voltage gain and does not require a rail to rail LO swing, preventing excessive consumption in the LO buffers. The used LO swing is around 300 mV peak to peak (single-ended), which is sufficient for the chosen circuit topology. Increasing the swing to 1 V, would result in an increase of the LO buffer power consumption by more than a factor of 9 (proportional to $V_{LO}^2$), hence justifying the choice of an active mixer. The transistor $M_1$ acts as a main transconductance stage, that converts the input voltage into current before the downconversion. Center-tapped symmetric inductor $L_1$ acts as a transformer and boosts the equivalent transconductance of transistor $M_1$ [2, 3], without the increase of power consumption, making this approach ideal for a low power design. Disregarding capacitor $C_T$ for the moment, and assuming $C_2$ is large enough to be considered as a short circuit at the frequencies of interest, the equivalent transconductance seen from the gate of $M_1$ is given by

$$G_{m,eq} = \frac{\Delta I_1}{\Delta V_G} = \frac{(k+1)G_{m1}}{1 + \mathrm{j}\omega L G_{m1}(1-k^2)}, \tag{5.1}$$

where $k$ is the transformer coupling coefficient. As $k$ approaches 1 (ideal transformer) the equivalent transconductance becomes purely real and equal to $2G_{m1}$. It has been shown that, for the same current consumption, this

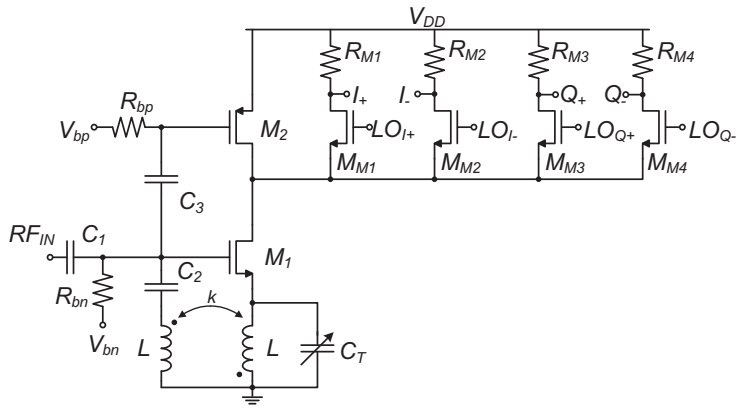



**Figure 5.2** Schematic of the LNA/Mixer.

approach achieves higher gain and larger bandwidth compared to the standard inductively degenerated LNA [3].

It was shown in [2] that the input impedance of the transformer feedback LNA is given by (assuming $C_2$ is large, $C_{GS} \ll C_1$, $k = 1$, $C_T = 0$ and $\omega^2 L^2 G_{m1}^2 \gg 1$)

$$Z_{in} \approx \frac{1}{\mathrm{j}\omega C_1} + \mathrm{j}\omega L + 2\omega^2 L^2 G_{m1}. \tag{5.2}$$

Resonance frequency is then $\omega_0^2 = 1/LC_1$. In this design, tuning capacitor $C_T$ is added to provide capability to tune the resonance frequency and to compensate for small component variations. With $C_T$ the expression of the input impedance becomes:

$$\begin{aligned} Z_{in} \approx \frac{1}{\mathrm{j}\omega C_1} &+ \mathrm{j}\omega L \frac{1-\omega^2 LC_T(2-k^2)}{1-2\omega^2 LC_T} \\ &+ \omega^2 L^2 G_{m1} k(1+k) \frac{1-\omega^2 LC_T(1-k)}{1-2\omega^2 LC_T}. \end{aligned} \tag{5.3}$$

In the above expression it is assumed that $C_T \ll C_1$, which means that close to resonance $\omega^2 LC_T < 1$. Assuming $k = 1$, 5.3 can be further simplified to:

$$Z_{in} \approx \frac{1}{\mathrm{j}\omega C_1} + \mathrm{j}\omega L \frac{1-\omega^2 LC_T}{1-2\omega^2 LC_T} + \frac{2\omega^2 L^2 G_{m1}}{1-2\omega^2 LC_T}, \tag{5.4}$$

which shows that the resonance frequency is now a function of $C_T$. Unfortunately, $C_T$ also affects the real part of the input impedance, however it is still possible to achieve good matching and roughly 10% tuning range of the resonance frequency.

A common problem in active mixers is that the bias current required by the transconductance $M_1$ and switching transistors $M_{M1-4}$ is not the same. Bias current of $M_1$ is set by the input matching condition and the desired voltage gain. Voltage gain of the active mixer is proportional to the product of the transconductance and the load resistance $G_{m1}R_{M1-4}$. At the same time, the dc point of the output voltage and the LO feedthrough ($\mathrm{I}_{+/-}$ and $\mathrm{Q}_{+/-}$ outputs) are dependent on the product of the bias current and load resistance $I_bR_{M1-4}$. Increasing the voltage gain, either through $G_{m1}$ (and consequently $I_b$) or through $R_{M1-4}$ lowers the output bias voltage and increases the LO feedthrough. To add a degree of freedom and break this dependence, "current stealing" technique can be used. This is accomplished using the transistor $M_2$, that sinks part of the $M_1$ bias current. In this way, mixer bias current can be set independently of the $M_1$ bias current, allowing to break the dependence between the voltage gain on one side and dc bias and LO feedthrough on the other. As a consequence, load resistor values can be increased to maximize voltage gain without causing excessive LO feedthrough. In addition to current stealing, since the gate of $M_2$ is connected to the LNA input through a large capacitor $C_3$, it also contributes to the overall transconductance, further increasing voltage gain. The approach is similar to the complementary LNA presented in [4], with the difference that the bias currents of $M_1$ and $M_2$ are not the same. The addition of $M_2$ has some downsides in a practical implementation. More complex layout of the LNA will result in increased parasitics, and more importantly drain capacitance of $M_2$ will be added to the parasitic capacitance at the mixer input, effectively reducing bandwidth of the RF front-end. To compensate for the added capacitance, the equivalent input resistance of the mixer can be reduced by increasing the size of the switching transistors $M_{M1-4}$, but this comes at price of increasing the load of the LO buffers.

In this design, resistors $R_{M1-4}$ can be switched between $22\,\mathrm{k\Omega}$ and $14\,\mathrm{k\Omega}$ and provide two gain steps for the mixer. Since the voltage gain is obtained entirely at baseband frequencies, after mixing, it comes at a lower cost in terms of power, and eliminates the need for a resonant load, thereby saving silicon area. Achieved voltage gain is around 15 dB over a 600 MHz bandwidth, for the maximum gain setting. Simulated current consumption is $70\,\mu\mathrm{A}$ from a 1 V supply. The input referred 1 dB compression point

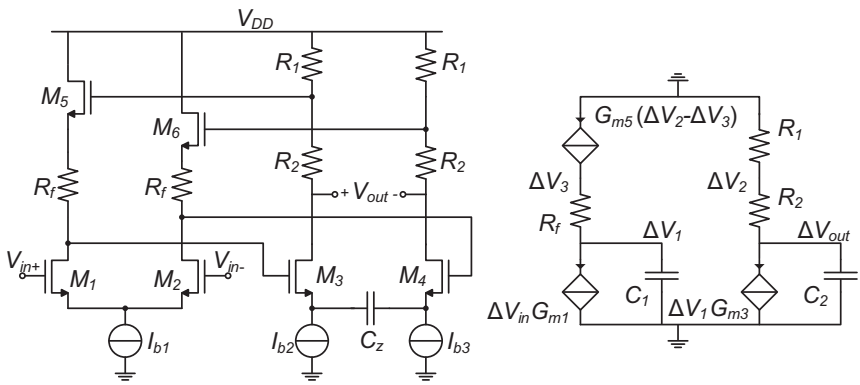



**Figure 5.3** Schematic of the IF amplifier, and the equivalent small-signal schematic of half circuit.

of the RF frontend is at $-19$ dBm. The price to be paid for low power consumption is elevated noise figure, which in this case is 15 dB according to simulations (this is including the LNA and the mixer). Even though it is higher than the typical values found in standard receiver implementations, it is still acceptable for communication over short distances.

### 5.3.2 IF Amplifier

The mixer is followed by the I and Q IF amplifiers that provide most of the voltage gain. Each IF amplifier is a cascade of three modified CMOS Cherry-Hooper (CH) amplifiers shown in Figure 5.3. The basic concepts that come from [5] were further developed in [6], where emitter-follower was introduced in the feedback, and the first CMOS version was presented in [7]. A CH amplifier is a feedback amplifier with a second order transfer function. Compared to a cascade of standard differential pairs, feedback amplifiers offer larger bandwidth for the same power consumption. This is why these amplifiers were originally used for high data rate optical receivers, targeting bandwidths of more than 1 GHz. In this case, the design was optimized for 300 MHz bandwidth and low power consumption. By controlling the Q-factor of the transfer function, behavior close to the edge of the pass-band can be controlled. In this particular case peaking was used to compensate for the slight drop in the LNA/mixer conversion gain close to the band edges and provide a relatively flat overall gain characteristic.

The small-signal schematic of the half-circuit is given in Figure 5.3. Capacitors $C_1$ and $C_2$ are a combination of gate capacitance (in the case

of $C_2$ this would be the gate capacitance of the following stage) and layout parasitics. Capacitance $C_z$ introduces a zero in the transfer characteristic, and is used to prevent offset accumulation in the IF amplifiers. Although, strictly speaking, the downconverted FM-UWB signal occupies frequencies from 0 to 250 MHz, a zero in the transfer function will not affect the performance of the demodulator as long as this zero is low compared to the signal bandwidth. In this case the zero is placed around 1 MHz, and since it will not affect the behavior in the pass-band it is not considered in the small-signal analysis. Gain in the pass-band is given by [7]:

$$A_{v0} = \frac{G_{m1}(R_1 + R_2)(1/G_{m5} + R_f)}{(1/G_{m3} + R_1)}. \tag{5.5}$$

Assuming $G_{m5}R_f \gg 1$ and $G_{m3}R_1 \gg 1$ the above expression reduces to

$$A_{v0} \approx \frac{G_{m1}(R_1 + R_2)R_f}{R_1}. \tag{5.6}$$

As the voltage gain is a function of the ratio of the two load resistors $R_1$ and $R_2$, gain switching can be implemented by switching the value of $R_2$. The second order transfer function of the CH amplifier is given by

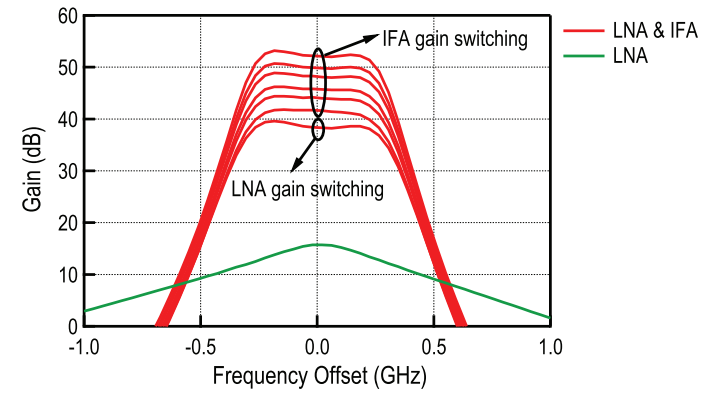
$$\begin{aligned} A_v(s) &= \frac{G_{m1}G_{m3}(R_1 + R_2)(1 + G_{m5}R_f)}{a + bs + cs^2}, \\ a &= G_{m5}(1 + G_{m3}R_1), \\ b &= (C_1(1 + G_{m5}R_f) + G_{m5}C_2(R_1 + R_2)), \\ c &= C_1C_2(R_1 + R_2)(1 + G_{m5}R_f). \end{aligned} \tag{5.7}$$

Again, assuming the transconductances are high enough that $G_{m5}R_f \gg 1$ and $G_{m3}R_1 \gg 1$ leads to the simplification of the expression that reduces to

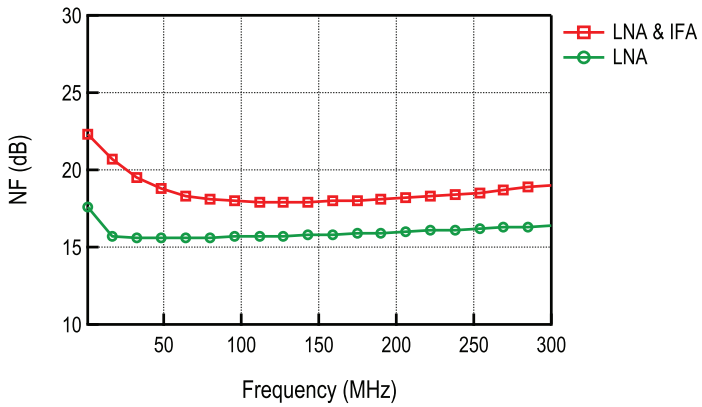
$$A_v(s) = \frac{G_{m1}G_{m3}(R_1 + R_2)R_f}{G_{m3}R_1 + s(C_1R_f + C_2(R_1 + R_2)) + s^2C_1C_2(R_1 + R_2)R_f}. \tag{5.8}$$

Capacitors $C_1$ and $C_2$ are determined by the size of the differential pair transistors and the layout parasitics. Gain, bandwidth and Q-factor of the amplifier transfer function are then set by the resistances of $R_1$, $R_2$ and $R_f$, which can be used as design parameters.

Simulated gain of the standalone LNA/mixer, and the LNA/mixer together with IF amplifiers is shown in Figure 5.4(a). Overall gain of all the




(a) Conversion gain




(b) Regenerative demodulator

**Figure 5.4** Simulated conversion gain and noise figure of the RF and IF stages.

stages preceding the FM demodulator is around 53 dB, with approximately 38 dB provided by the IF amplifier. Each CH amplifier cell requires 20 $\mu$A of current, which results in 120 $\mu$A consumed by the I and Q IF amplifier chains. Equivalent 6th order filtering characteristic provides the attenuation of 32 dB at an offset frequency of 500 MHz. Gain control is implemented through switching of $R_2$, that can take one of the values 6 k$\Omega$, 18 k$\Omega$ and 30 k$\Omega$, while $R_1 = 24\,\text{k}\Omega$. With three cascaded stages, the designed IF amplifier provides 6 different gain levels and one additional level is provided by switching the mixer load resistors $R_{M1-4}$. Different gain levels can be seen in Figure 5.4(b). Figure 5.4(b) shows the simulated noise figure of the

standalone RF frontend and of the RF frontend and the IF amplifiers together. The RF frontend provides around 15 dB of voltage gain, however the power remains low. This is a consequence of low bias current of the LNA/mixer, that results in a low value of transconductance. As a result, the noise added by the IF amplifiers will increase the total noise figure by approximately 3 dB. The noise figure of the standalone IF amplifier is around 5 dB in the pass-band. Finally, even though the noise figure is higher compared to more conventional receiver implementations, the achieved levels still provide enough sensitivity for communication over short distances.

### 5.3.3 LO Generation and Calibration

The proposed receiver is intended for use in the lower part of the UWB band, targeting 500 MHz wide signal centered around 4 GHz. The emphasis of the work described here is on reducing the power consumption of the receiver, while still preserving the capability to operate in an environment where several FM-UWB transceivers might be communicating at the same time. The power reduction dominantly comes from the fact that the gain stages operate at low frequencies, while no voltage gain is provided at RF. However, such an approach can only be beneficial if the LO signal can be generated efficiently. Additional difficulty is the need for quadrature signals since a $90^\circ$ shift is generally required for correct demodulation in a direct conversion (zero IF) receiver. Providing such signals at 4 GHz tends to be power costly. Fortunately, owing to the properties of FM-UWB and the chosen receiver architecture, the oscillator constraints are quite loose. Due to the large bandwidth of the FM-UWB signal, phase noise is not a major concern ($-80$ dBc at 10 MHz offset according to [8]) and no precise frequency generation is needed, therefore a simple free-running ring oscillator can be used to provide carrier signals for downconversion. When it comes to power consumption, ring oscillators are advantageous compared to LC oscillators, as they benefit from technology scaling. Inductor quality factor, which is a limit to power consumption of integrated LC oscillators, remains constant and practically independent of technology. On the other hand, gate capacitance and interconnect parasitic capacitances, that determine consumption of ring oscillators, decrease with technology scaling. This enables the reduction of power consumption of the ring oscillator, making the proposed approach favorable for future implementations.

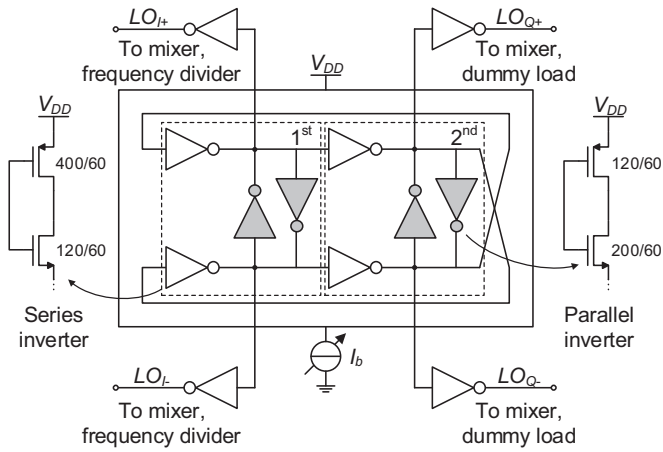



**Figure 5.5** Simplified schematic of the quadrature DCO.

The oscillator schematic is shown in Figure 5.5. A chain with an even number of inverters is needed to provide quadrature signal generation, however such a circuit would latch on its own. In order to prevent latching, and force a $180^\circ$ phase shift, parallel inverters are added between the corresponding nodes (grey inverters in Figure 5.5). A different way to see the implemented oscillator would be as a pseudo-differential two stage ring oscillator, where each stage consists of four inverters and the differential mode is enforced by the parallel inverters [9, 10]. The two stages provide a $90^\circ$ phase shift, and an additional $180^\circ$ shift is provided by cross-coupling the stages, hence assuring a reliable start-up. The series and parallel inverters are sized differently, W/L ratios in nm are shown in Figure 5.5, dimensions were optimized for low power consumption. One of the difficulties in designing very low power ring oscillators is that capacitive load is dominantly determined by the capacitance of the interconnect wires, and is layout dependent. Careful layout design with several iterations is needed to minimize power consumption. Correct phase relations between different signals are guaranteed by symmetry, however a small quadrature error is present due to mismatch between transistors. The error will vary from die to die and according to Monte Carlo simulations their standard deviation is $\sigma_\phi = 2.6^\circ$. Frequency is controlled via supply current of the current starved CMOS inverters. All inverters share the same current source as this approach was proven to perform better than the solution with a separate current source for each inverter, or inverter pair [9].

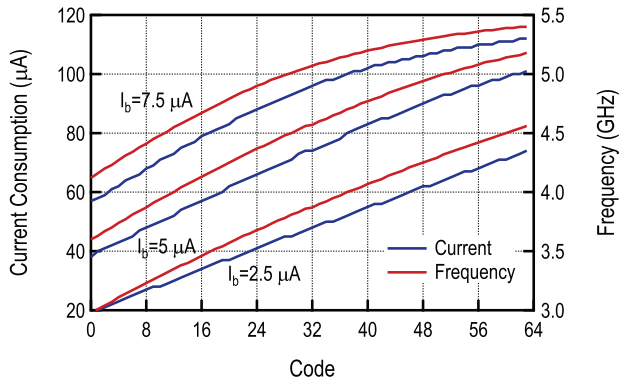



**Figure 5.6** Simulated frequency and current consumption of the DCO.

Since process-voltage-temperature (PVT) variations can have a significant impact on the oscillation frequency, the digitally controlled oscillator (DCO) was designed to cover the frequency range from 3 GHz to 5 GHz, thus assuring that it can be tuned correctly under all conditions. A 6-bit current DAC is used to provide the supply current, resulting in less than 30 MHz frequency resolution. The frequency step is not constant due to nonlinear characteristic of the DCO and decreases as the oscillation frequency increases. At 4 GHz the DCO produces a 300 mV peak-to-peak single-ended signal while consuming 140 $\mu$A (including the buffers). Simulated oscillation frequency and current consumption of the DCO, as functions of input code, are shown in Figure 5.6 for different DAC reference currents.

Since the oscillation frequency of the DCO is imprecise and prone to environment changes it must be calibrated periodically to assure correct operation (e.g. to compensate for temperature). Since environmental changes are slow, the calibration would only need to be done once in a few hours or potentially even days, meaning that the consumption of the calibration circuitry on average remains negligible compared to the receiver consumption. The calibration can be done using a frequency-locked loop (FLL) that is turned on as needed. The FLL was not integrated in this implementation, however it can be added externally using a microcontroller or an FPGA, and the available output from the on-chip frequency divider. A fixed ratio, integer frequency divider is implemented as a cascade of 10 divide-by-2 cells. By selecting outputs from different dividers, one of the four divide ratios 128, 256, 512 and 1024 can be selected as an output for calibration. Each cell is a simplified version of a dynamic 2/3 divider circuit described in [11]. It was designed to cover a somewhat larger range of frequencies than the DCO

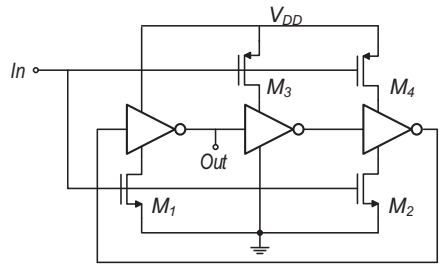



**Figure 5.7** Schematic of the frequency divider.

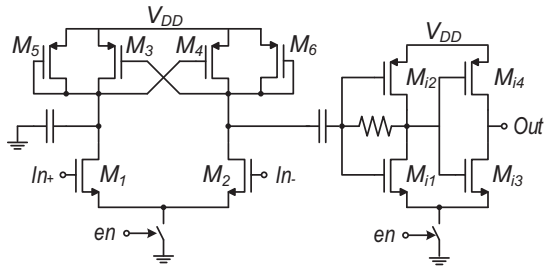



**Figure 5.8** Schematic of the buffer between the DCO and the frequency divider.

to assure reliable operation. Owing to the simplified structure, the circuit from Figure 5.7 can work up to 6 GHz. Since the divider requires a rail-to-rail input signal, it is preceded by a buffer from Figure 5.8 that performs differential to single-ended conversion and amplifies the signal. The first stage of the buffer is a pseudo-differential amplifier that uses positive feedback to boost the gain. The positive feedback is implemented using the cross-coupled transistors $M_3$ and $M_4$ that provide a negative transconductance. This negative transconductance is used to minimize the equivalent output conductance of the amplifier and increase gain. The differential amplifier is followed by inverters that further amplify the LO signal and produce a rail-to-rail voltage at the output. The whole buffer consumes around 250 $\mu$W at 4 GHz and its power consumption is proportional to the input frequency. Figure 5.9 shows simulated waveforms at the buffer input and output, and divider signals in different points. The whole divider chain consumes around 150 $\mu$W, and the largest part of the consumption is coming from the first two stages that operate at the highest frequencies.

The frequency divider buffer itself is connected to the $LO_{I+}$ and $LO_{I-}$ outputs of the DCO buffers. Dummy load is added to $LO_{Q+}$ and $LO_{Q-}$ to prevent amplitude mismatch between the I and Q LO signals. Even though

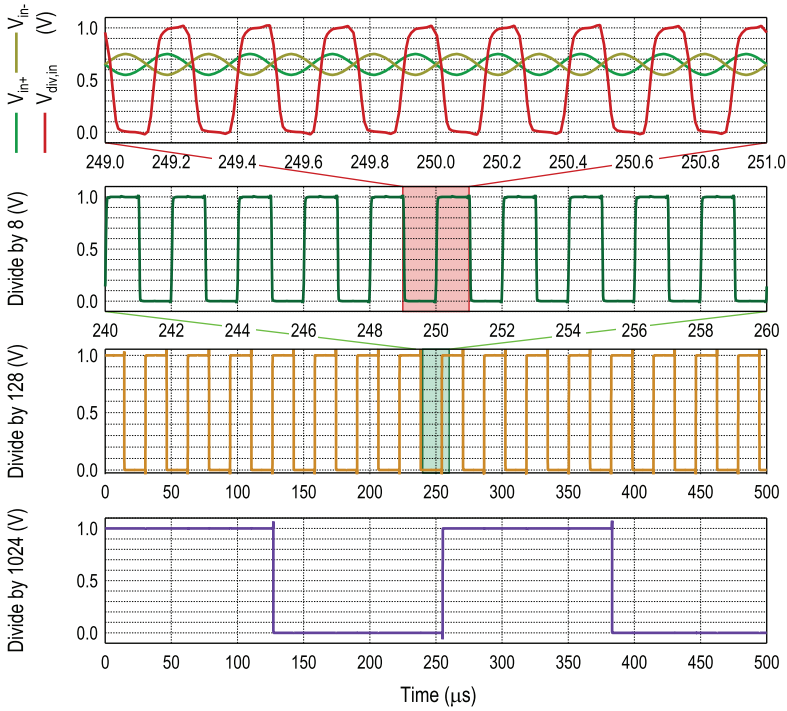



**Figure 5.9** Frequency divider, waveforms at different points.

the DCO itself can produce a sufficiently large output amplitude, the four buffers (Figure 5.5) need to be placed between the internal nodes of the DCO and the inputs of the mixer and divider. This is done to decouple the oscillation frequency from the mode of operation (reception or calibration). The input capacitance of the divider buffer varies with the bias current of the two input transistors, and is different in the on and off state. If these buffers were connected directly to the DCO, the change in load capacitance would cause a shift in frequency after calibration. In addition, the presence of DCO buffers reduces coupling between the external signal and the DCO, thus preventing the pulling effect (shift in frequency caused by external signal). The four buffer inverters consume around 80 $\mu$A, almost 60% of the entire DCO consumption which is a significant but necessary overhead.

### 5.3.4 FM Demodulator

The implemented wideband FM demodulator is a modified version of the delay-line demodulator presented in [1]. In order to conserve power, the demodulator has been moved from RF to baseband, but it now requires quadrature inputs to perform correct FM demodulation. Additional benefit of moving the demodulator to baseband is that there is no need for precise delay generation, as it is no longer related to the input signal frequency. The only limit is coming from the demodulator bandwidth that is inversely proportional to the delay. The implemented delay-line demodulator is presented in Figure 5.10. Two double-balanced Gilbert's mixers perform multiplication of the I and Q signals with their delayed copies. The output currents of the two cells are combined to implement subtraction and produce the demodulated signal. Top inputs of Gilbert's mixer are connected directly to the outputs of the IF amplifier (gates of transistors $M_{3-6}$). Source followers are placed between the IF amplifier and bottom inputs (gates of transistors $M_{1,2}$) to provide a correct dc level of the input voltage. The delay path consists of source followers $M_{SF1,2}$ and bottom transistors of the Gilbert's mixer $M_{1,2}$. For a first order filter with a pole at $\omega_p$ it can be shown that the delay through the filter is equal to $1/\omega_p$, for a signal whose maximum frequency is sufficiently below the cut-off frequency. In this case the total delay is a sum of delays that come from two poles. The first one is associated to the source

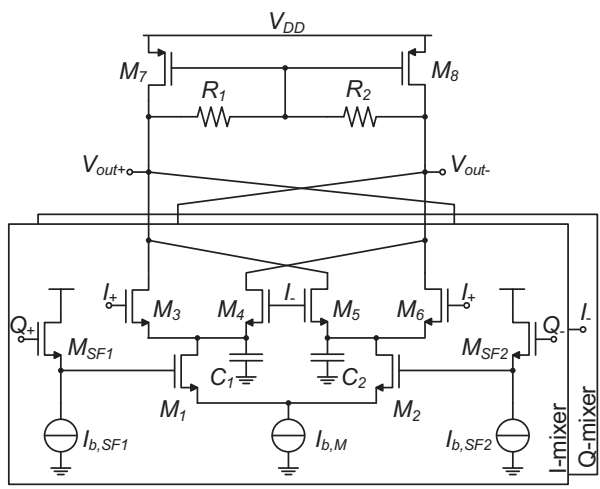



**Figure 5.10** Schematic of the wideband FM demodulator.

follower and is given by

$$\tau_1 \approx \frac{C_{G1}}{G_{m,SF1}}, \tag{5.9}$$

where the capacitance $C_{G1}$ accounts for the total capacitance seen at the gate of $M_1$. Since $M_1$ is a relatively small transistor, parasitics will contribute a significant portion of the total load.

Due to the asymmetry of the double balanced mixer with respect to the two signal paths, some delay will inherently exist between the bottom and top inputs. This delay is caused by the pole that exists due to the parasitic capacitance at the drain of $M_1$. To provide better control of the delay and reduce dependence on parasitics, an additional MOM (metal-oxide-metal) capacitor is added in this node ($C_{1,2}$), resulting in the delay that is given by

$$\tau_2 \approx \frac{C_1}{G_{m3} + G_{m4}}. \tag{5.10}$$

All the transistors in the FM demodulator are biased in weak inversion. Since the transconductance of each transistor is proportional to the bias current, delay of the demodulator can consequently be controlled by the bias currents $I_{b,SF}$ and $I_{b,M}$. Two bit control of the bias current is provided to allow delay tuning after production. Load resistors $R_1$ and $R_2$ can be switched between the two values to provide two gain settings. The FM demodulator input and output waveforms are shown in Figure 5.11. The figure shows the input sub-carrier signal (top), the I and Q signals (middle) and the demodulated signal (bottom). A small distortion can be seen at the peak values of the demodulated signal. This is a result of the IF amplifier bandwidth, combined with the fact that delay decreases at higher frequencies.

The demodulator consumes only 25 $\mu$W, mainly due to the fact that it operates at baseband. Compared with the demodulators from [12, 13], that require close to 6 mW, this is an improvement by two orders of magnitude, allowing significant power savings and still providing sufficient linearity to handle multiple input FM-UWB signals. Additionally, there is no need for inductors and no need for a complex passive network that provides a precise delay, thus resulting in area savings as well.

### 5.3.5 LF Amplifier and Output Buffer

For the targeted sensitivity levels, the signal amplitude at the output of the demodulator will be too low. Before it can be digitized and analyzed, the

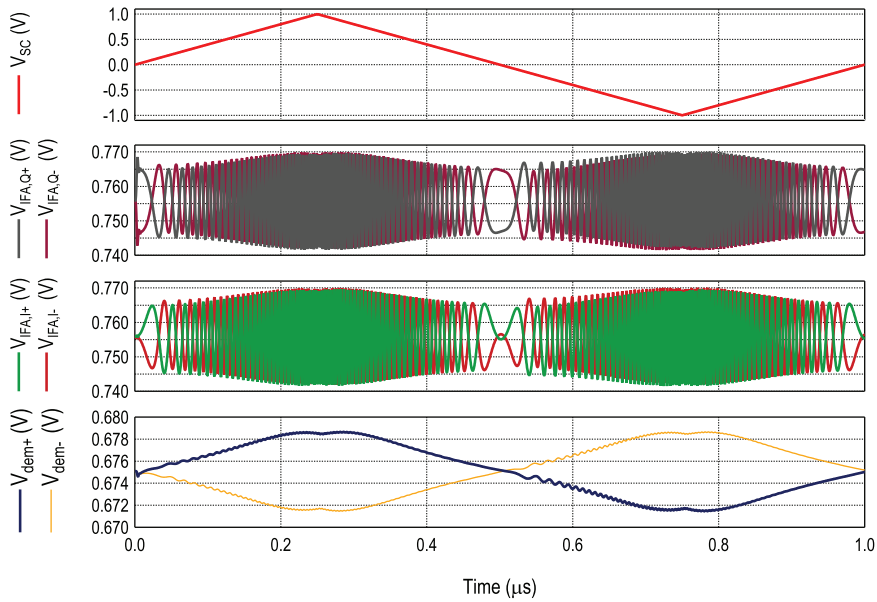



**Figure 5.11** Wideband FM demodulator, input and output waveforms.

signal must be amplified and filtered. The two low-frequency (LF) amplifiers that follow the FM demodulator provide a band-pass characteristic from 1 MHz to 2.5 MHz and a maximum voltage gain of roughly 20 dB while consuming 15 $\mu$A. As shown in Figure 5.12, each stage is implemented as a fully differential amplifier with resistive source degeneration. Source degeneration provides better linearity, and more precise gain control. The gain of the amplifier is given by

$$A_v = -\frac{G_{m1}R_L}{1+G_{m1}R_S/2} \approx -\frac{R_L}{R_S/2}. \tag{5.11}$$

The approximation is valid if $G_{m1}R_S/2 \gg 1$, in which case the gain is solely determined by the ratio of load and source resistors. Two bit gain control is provided, both $R_L$ and $R_S$ can be switched between the two values. Since the higher cut-off frequency is determined by $R_L$ and the capacitance loading the amplifier output (gate capacitance of the following stage in series with $C_{ac}$), decreasing the gain also extends bandwidth. The lower cut-off frequency is determined by the elements of the ac coupling network as $1/R_bC_{ac}$.

Source followers $M_{o1}$ and $M_{o2}$ are placed at the output to provide a low impedance stage that drives the external circuits. They are design to drive

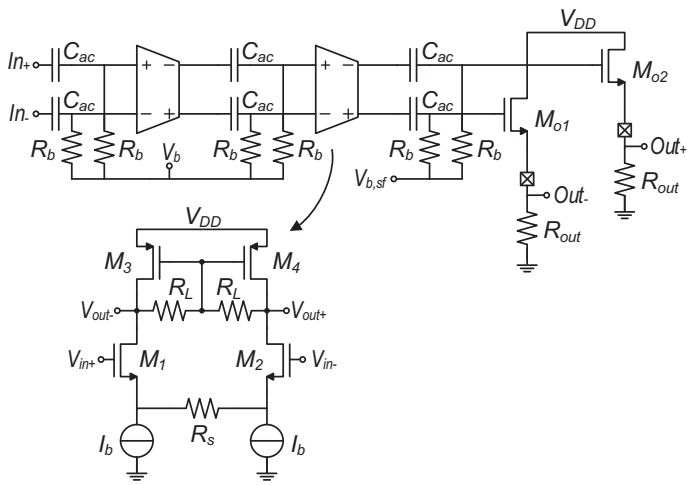



**Figure 5.12** Schematic of the output buffer.

a load of 10 pF, which corresponds to the capacitance of the oscilloscope probes or an external ADC, used to digitize the signal, although if necessary an additional external buffer can be added. External resistors define the bias current of the source followers, and can be chosen to have any value between 1 kΩ and 10 kΩ, while still providing sufficient bandwidth.

### 5.3.6 Current Reference PTAT Circuit

All the circuits described so far require a reference current that defines the bias point. All the reference currents are derived from a single current generated by the circuit from Figure 5.13. The circuit provides a PTAT (proportional to absolute temperature) reference current and reuses the approach from [14]. It is a closed loop circuit made up of two current mirrors, a 1:1 current mirror $M_5$–$M_6$ and a 1:$K$ current mirror $M_1$–$M_2$. Transistors $M_3$ and $M_4$ are used as cascode transistors that define the drain voltage of $M_1$ and $M_2$. The bias current is defined by the ratio of $M_1$ and $M_2$, and since they are both biased in weak inversion the generated reference current $I_{out}$ is given by

$$I_{out} = \frac{U_T \ln K}{R}. \tag{5.12}$$

The output current is proportional to absolute temperature through thermal voltage $U_T = kT/q$. The generated current is used as a reference current

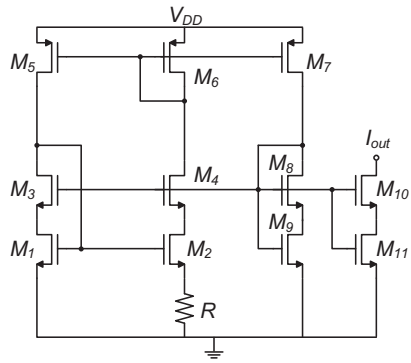



**Figure 5.13** Schematic of the PTAT current reference.

for an array of current DACs that provide a reference current for each block of the system. Each of the reference currents can be digitally controlled with a resolution of 1.25 $\mu$A, allowing some room for adjustment of the bias current after production.

## 5.4 Measurement Results

### 5.4.1 General Receiver Measurements

The proposed receiver was integrated in a standard 65 nm bulk CMOS process. The die photograph is presented in Figure 5.14. The active area of the receiver is approximately 0.4 mm$^2$, including roughly 450 pF of decoupling capacitance. The receiver only requires one inductor, with no additional off-chip components, which results in smaller area than most existing

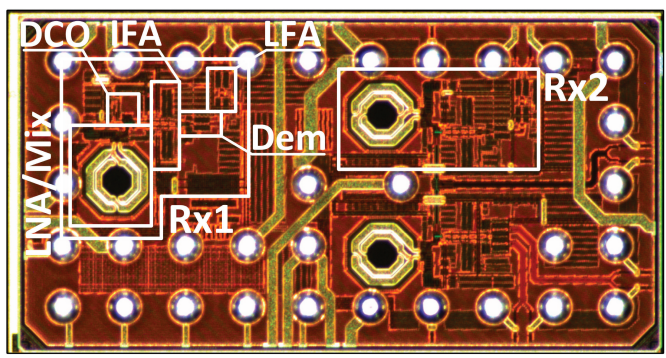



**Figure 5.14** Die photograph.

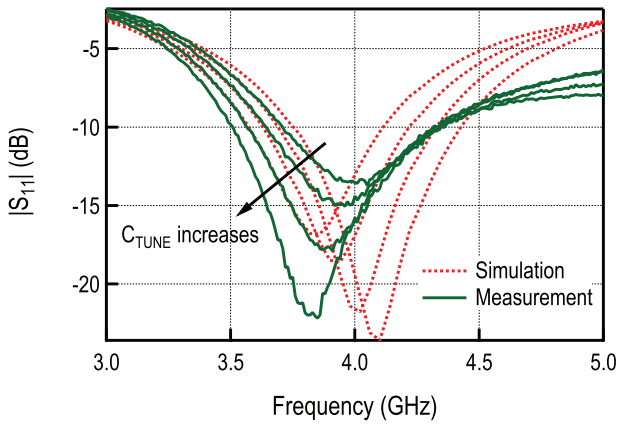



**Figure 5.15** Measured $S_{11}$ parameter for different values of input capacitance.

implementations. As already mentioned, two receivers were implemented on the same die for testing purposes. Rx1 is the main receiver that uses the ring oscillator described in the previous section to generate the quadrature LO signals. Rx2 is the test receiver that is identical to the first receiver except that it uses an externally generated LO signal. Two input pads are used for the differential LO, and the on-chip RC-CR network produces quadrature signals. The test receiver is integrated to serve as a reference that allows assessment of performance degradation due to a non-ideal locally generated carrier signal.

Figure 5.15 shows the simulated and measured $S_{11}$ parameter of the receiver for different values of tuning capacitor $C_T$. A small difference in measured and simulated values is observed. The measurement was done on an FR4 test board with a 10 mm long 50 Ω coplanar waveguide between the pad and the connector. This line was not taken into account in the simulations and might be the cause of the shift in the resonance frequency. Nevertheless, the reflection coefficient is below −10 dB in the band of interest, providing sufficiently good matching.

The DCO frequency was measured using the on-chip frequency divider. As shown in Figure 5.16 the oscillation frequency can be varied from 3.1 GHz to 4.7 GHz. At the same time the supply current of the DCO changes from 32 $\mu$A to 85 $\mu$A. At 4 GHz the DCO consumes around 60 $\mu$A, while the buffer consumes an additional 80 $\mu$A, a consequence of the fact that differential quadrature signals need to be buffered. Only one die measurement is presented here, however the frequency characteristic will vary significantly from one die to another as a result of process variation. Nevertheless, all of the measured dies covered the range from 3.6 GHz to 4.4 GHz and could be

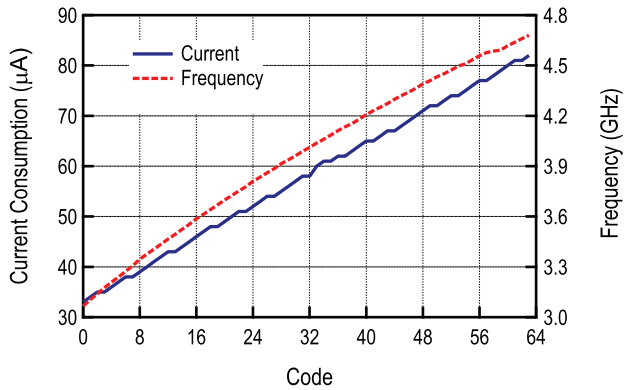



**Figure 5.16** Measured frequency and current consumption of the DCO.

**Table 5.1** Power consumption breakdown

| Block | Current Cons. ($\mu$A) | Relative Cons. (%) |
|---|---|---|
| LNA & mixer | 91 | 21.5 |
| DCO & buffers | 140 | 33.1 |
| IF amplifier | 122 | 28.8 |
| Demodulator | 26 | 6.1 |
| LF amplifier | 15 | 3.5 |
| Bias | 29 | 6.9 |

calibrated properly. In all cases the power consumption remains practically the same for the DCO oscillating at 4 GHz. A slightly non-linear behavior can be observed in the output frequency, which is of no significance in this case since the only requirement for the calibration loop is monotonicity, which is satisfied.

The proposed receiver consumes 423 $\mu$W of power from a 1 V supply. Power breakdown is shown in Table 5.1. The highest consumer is the DCO together with buffers, followed by the IF amplifiers and the LNA. The demodulator, with only 26 $\mu$W of power consumption consumes two orders of magnitude less power than the same type of demodulators implemented previously in [12, 13].

### 5.4.2 Single User Measurements

The test setup used for the bit error rate (BER) measurements is presented in Figure 5.17. A random bit sequence is generated by software and mapped to the corresponding quadrature FM-UWB symbols. A 12 GS/s, 12-bit arbitrary waveform generator, M8190A was used to generate the baseband quadrature

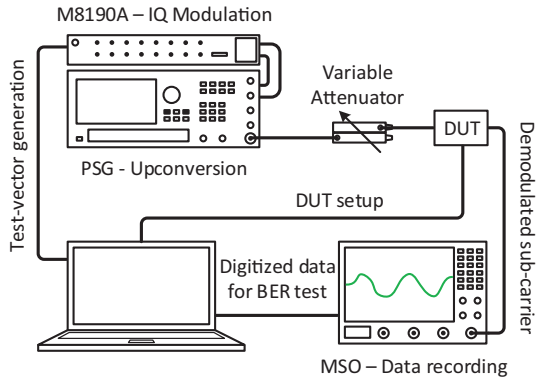



**Figure 5.17** Measurement setup.

FM-UWB signals. These signals are subsequently up-converted to 4 GHz by the Keysight PSG signal generator and used for receiver characterization. The flexibility provided by the M8190A allows to generate FM-UWB signal with different characteristics. Measurements with different data rates as well as with different modulation orders are reported in this section. The generator is also capable of producing different scenarios, that include multiple FM-UWB signals in the same RF band, but using different sub-carrier frequencies. The waveforms for different scenarios, as well as the test vectors for the BER measurements are generated using a PC. The same PC is then used to compare the original test vector with the demodulated data recorded by an oscilloscope, and finally produce the BER curves.

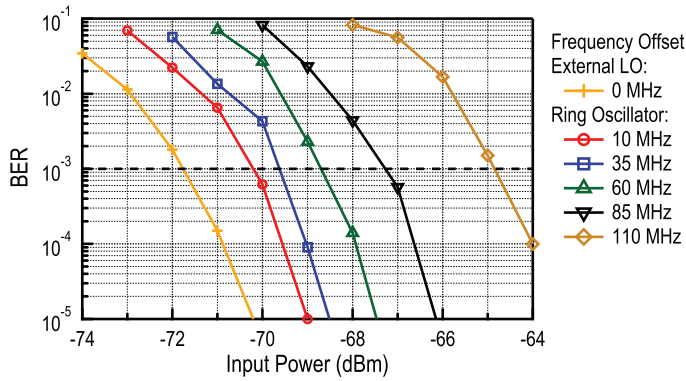
The on-chip demodulator performs the first, wideband FM demodulation, and provides the FSK sub-carrier at the output. The second FSK demodulation is performed by software. The receiver output signal is first recorded and digitized using the MSO oscilloscope (that acts as a 10 bit 20 MS/s ADC). The recorded vector is then demodulated using software. The FSK demodulator is implemented as a correlator, which is an optimal maximum-likelihood detector for this case.

As explained previously, two receivers were implemented on the same die in order to compare the receiver performance with the ideal LO and the integrated ring oscillator. Tests were performed using a nominal data rate of 100 kb/s, and the sub-carrier modulation index of 1, meaning that the frequency deviation from center frequency is $\Delta f = 50$ kHz. This is the minimum frequency deviation that preserves orthogonality between the two FSK frequencies for the case of non-coherent signaling. The BFSK

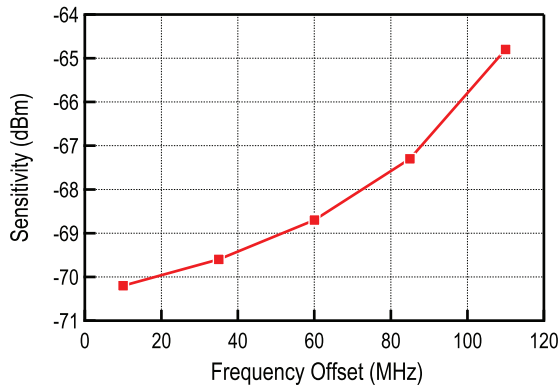
sub-carrier signal is not filtered (no pulse shaping is applied), which simplifies the receiver implementation but causes higher ACLR. For this measurement the sub-carrier signal is centered at 1.55 MHz, resulting in two sub-carrier frequencies at 1.5 MHz and 1.6 MHz, although different center frequencies could have been used as well.

In all cases, FSK frequencies are selected so as to have a continuous phase FSK signal. This is generally prefered in order to avoid discontinuities in the signal driving the VCO on the transmitter side, and is therefore used for testing. Sensitivity is defined as the input power that provides a BER of $10^{-3}$. The result is shown in Figure 5.18. Measured sensitivity of the receiver with an external LO signal is around $-72$ dBm. The approximate calculation presented by Gerrits in [1] suggests a sensitivity of $-78$ dBm for the noise figure of 18 dB. The difference is a result of imperfections present in the implemented receiver, most likely lower gain and increased noise figure of the RF frontend compared to the values obtained by simulation. The measured sensitivity with the internal ring oscillator is $-70$ dBm, a value approximately 2 dB worse than the sensitivity of the receiver with the external LO. This difference is a result of several factors. First, due to the limited frequency resolution of the internal DCO, it can never be configured to generate the carrier at exactly 4 GHz, meaning that a slight frequency offset will always be present. In this case, the minimum offset that could be achieved was 10 MHz. The second factor that deteriorates the sensitivity is the phase noise of the ring that after demodulation translates into the amplitude noise of the sub-carrier signal and degrades the SNR. The third factor is the amplitude of the LO signal. In the case of an external LO it was increased to provide the best achievable performance. The amplitude was set to 600 mV peak-to-peak at the receiver LO inputs, which results in approximately 420 mV after the RC-CR circuit. This value is larger than the simulated 300 mV peak-to-peak amplitude, that could be generated by the internal LO. The resulting difference is a small price to pay in order to reduce the power of the DCO, although it still remains the most power-hungry block in the receiver.

Additional degradation of sensitivity is expected as the frequency offset increases, as depicted in Figure 5.18(b). Each BER curve was measured after incrementing the DCO control word, roughly corresponding to 25 MHz increase in frequency offset. As shown in the previous chapter, the demodulator conversion gain decreases with the increase of the frequency offset. This effect is further emphasized by the finite bandwidth of the IF amplifier that attenuates the signal amplitude at the edges of the band for a frequency offset above 50 MHz. The effect can be observed in the output waveforms, shown in




(a) BER curves for different carrier offset




(b) Sensitivity vs. carrier frequency offset

**Figure 5.18** Measured BER curves for different carrier offset.

Figure 5.19. As the frequency offset increases the demodulated signal further deviates from the sine wave, thus increasing the power contained in the higher harmonics. The final result is the sensitivity degradation of about 5 dB for the frequency offset of 110 MHz. Depending on the maximum sensitivity degradation that can be allowed, the maximum tolerable frequency offset can be defined, which then translates into the maximum period between the two calibrations and the power overhead due to calibration [15].

Although different receiver architectures have been explored, most of them focused only on standard 2-FSK sub-carrier modulation, targeting data

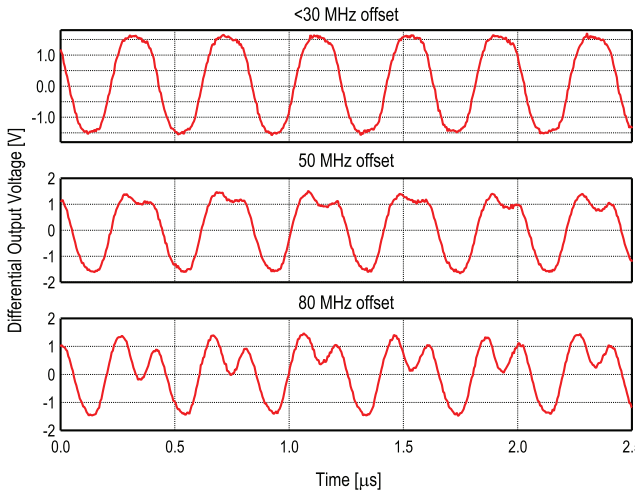



**Figure 5.19** Measured demodulator output waveform for different carrier frequency offsets.

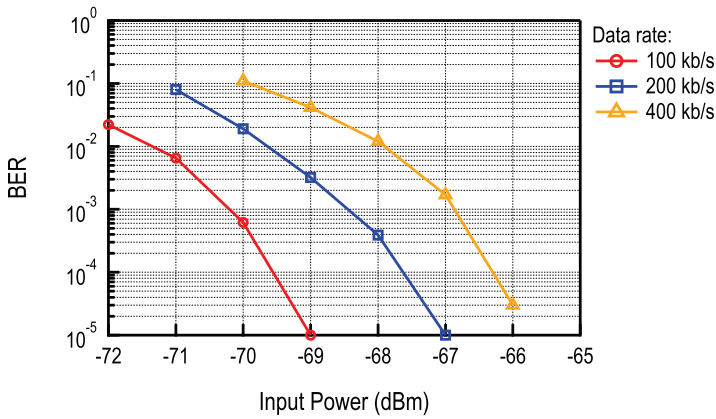



**Figure 5.20** BER curves for different data rates.

rates of 100 kb/s and below. Transmitters proposing higher data rates and higher order M-FSK modulations have been implemented, but the full communication with one of the existing receivers has never been demonstrated. In principle, any kind of modulation can be combined with wideband FM modulation to produce the FM-UWB signal. The proposed receiver can then be used to perform the first FM demodulation, while the subsequent sub-carrier demodulation is performed digitally, by software. Two cases are

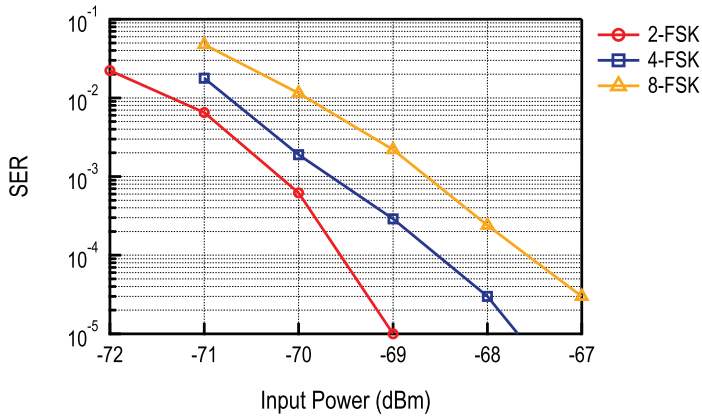
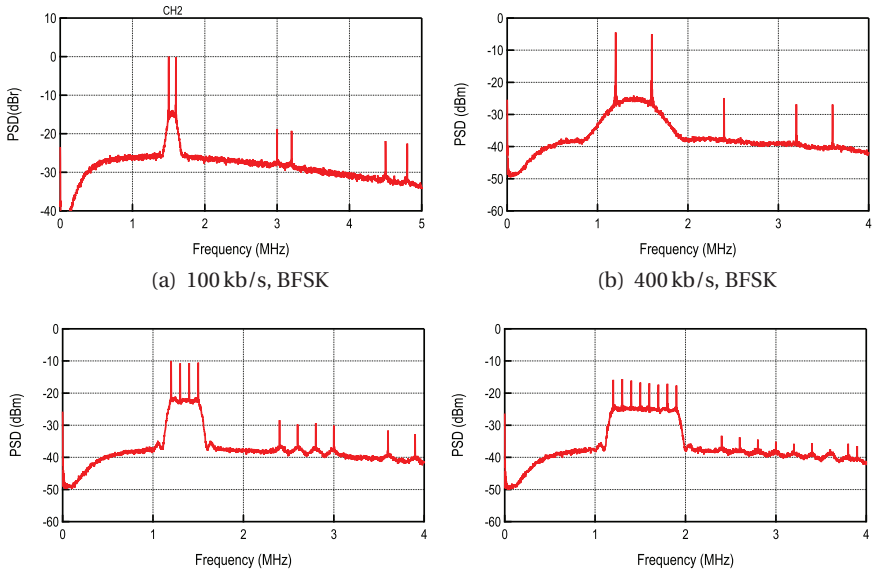



**Figure 5.21** BER curves for different modulation order.

of interest here, first is increasing data rate, and second is increasing the modulation order.

The BER curves for different data rates are shown in Figure 5.21. In all cases orthogonal, continuous phase FSK modulation is used. Modulation index is kept constant at 1, meaning that the frequency deviation and the sub-carrier bandwidth increase proportionally to data rate. The limit for the implemented receiver is coming from the bandwidth of the LF amplifier that was intended for operation from 1 MHz to 2.2 MHz. It could easily be extended, at an almost negligible increase in power consumption, if higher data rates are needed. In this case, the receiver is tested up to 400 kb/s. As expected, the sensitivity degrades as the data rate increases, but at a slower rate than in the case of narrow-band modulations, where doubling the data rate results in sensitivity shift of 3 dB. This is a consequence of the non-linear wideband FM demodulator characteristic and is typical for FM-UWB.

Measurements in Figure 5.21 show symbol error rate (SER) results for different FSK modulation orders. The equivalent BER depends on the used coding scheme, and should always be better than the SER. Assuming the same equivalent data rate, increasing modulation order leads to better performance in terms of equivalent BER. This comes at a price of increased sub-carrier signal bandwidth, and demodulator complexity that grows exponentially with the number of bits per symbol. In the reported measurements, the symbol rate is kept constant at 100 ksym/s, leading to 200 kb/s for 4-FSK and 300 kb/s for 8-FSK modulation. Figure 5.22 shows the sub-carrier spectrum at the output of the FM demodulator, shape and bandwidth depend




(a) 100 kb/s, BFSK (b) 400 kb/s, BFSK

(c) 200 kb/s, 4-FSK (d) 300 kb/s, 8-FSK

**Figure 5.22** Spectrum of the demodulated sub-carrier signal.

on the modulation order and data-rate. In principle, the proposed FM-UWB receiver could use different modulations and data rates to conform to channel conditions (e.g. if path loss is low, higher throughput can be achieved) and available sub-carrier bandwidth, and optimize network performance.

The FM-UWB modulation scheme inherently provides some robustness against narrow-band interferers. In the process of demodulation, the interferer itself is transformed into a dc component that can be filtered out. The cross product of the interferer and the FM-UWB signal results in a component that is spread over a large bandwidth and effectively increases the noise floor at the receiver output [1]. The performance of this receiver in the presence of a narrow-band interferer is shown in Figure 5.23. Sensitivity slowly degrades with the increase of interferer power up to $-48$ dBm. After that point, the interference becomes the dominant factor that causes erroneous reception and sensitivity begins to degrade linearly with the interference power. The lowest SIR that can be tolerated by this receiver is $-17$ dB (at $-48$ dBm interferer power) for an interferer frequency offset of 100 MHz from the center frequency.

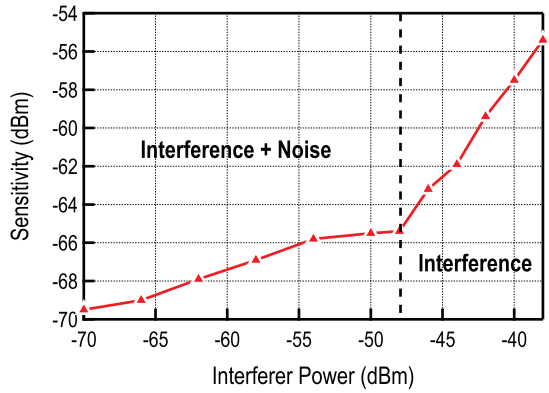



**Figure 5.23** Sensitivity as a function of in-band interferer power.

### 5.4.3 Multi-User Measurements

As shown previously, multiple FM-UWB signals transmitted in the same RF band can be demodulated simultaneously as long as the sub-carrier frequencies are different. At the demodulator output, the FSK modulated useful components will be found along with the spread component that is a result of the cross product between two or more FM-UWB signals. Unlike the useful components that can be filtered out in the baseband, the spread component will always be present and will cause the degradation of sensitivity as the power or number of interfering FM-UWB signals increase. The BER curves in the case of two FM-UWB users are presented in Figure 5.24. The measured sub-carrier channel is the same as in the single user case, centered at 1.55 MHz. Same parameters were used for both channels, 100 kb/s data rate and modulation index of 1, corresponding to sub-carrier bandwidth of 200 kHz. The interfering channel is centered at 1.25 MHz, which provides 100 kHz spacing between the two sub-carrier channels to avoid excessive ACPR. As expected, sensitivity decreases with the increasing power of the interfering FM-UWB signal. The quadratic characteristic of the demodulator will cause the sensitivity degradation to occur quite rapidly. As an example, a 3 dB stronger interferer at the RF input results in 6 dB stronger FSK sub-carrier in the baseband. In order to tolerate significant difference of power levels, high dynamic range baseband circuitry would be needed together with sharp channel filtering. In this case, channel filtering is performed in the digital domain, using a band-pass FIR filter. Since the interfering signals are not filtered before the analog to digital conversion, receiver dynamic range is limited by the dynamic range of the output buffer. Instead of increasing

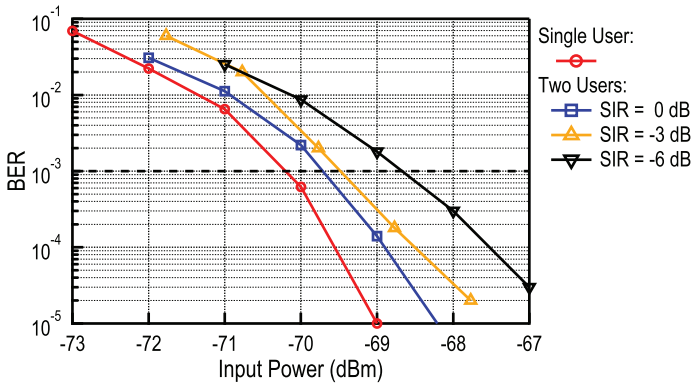



**Figure 5.24** BER curves for 2 FM-UWB users and varying input level between the two users.

the dynamic range of the receiver, which would inevitably result in increased power consumption, the problem could be approached at the protocol level by regulating the power on the transmitter side. For the case of HD-WSNs, this approach should not carry too much overhead in terms of complexity as the nodes should not move significantly relative to each other (in comparison with, for example, CDMA in the cellular network).

Just like the inter-user interference increases with the increasing power of the second FM-UWB signal, the increasing number of FM-UWB users will also increase the inter-user interference [16]. Figure 5.25 shows the scenario where the number of users increases from 1 to 4, while the power remains equal in all the channels. The increasing number of channels leads to degraded sensitivity and, just as in the previous case, requires larger dynamic range. Limiting factors to the number of channels, are sub-carrier frequencies, ACLR, channel separation, dynamic range, data rate and inter-user interference. For the given system parameters, 200 kHz wide channels with 100 kHz channel spacing, a maximum of four channels can be used if the lowest sub-carrier channel is located at 1.25 MHz. The demodulator output spectrum is presented in Figure 5.26 for different multi-user scenarios. The measured channel (channel 2, centered at 1.55 MHz) is highlighted in green, and the interfering channels are highlighted in red. A different number of occupied channels can be observed in different figures. As suspected, it can be seen that the spectrum above 2.3 MHz is polluted by the harmonics of the sub-carrier signals and intermodulation products, thus preventing the placement of additional channels in this band. The harmonics

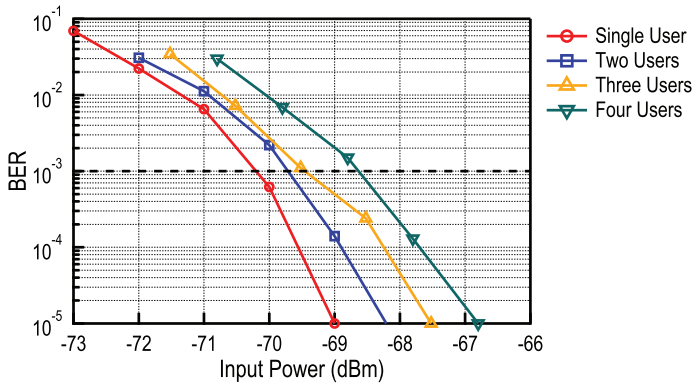
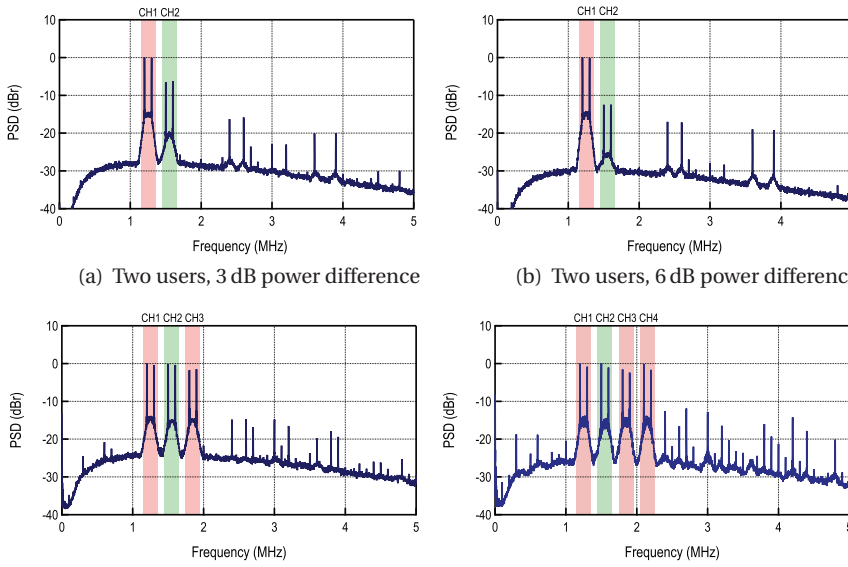



**Figure 5.25** BER curves for different number of FM-UWB users.




(a) Two users, 3 dB power difference

(b) Two users, 6 dB power difference

(c) Three users, equal power

(d) Four users, equal power

**Figure 5.26** Spectrum of the demodulated sub-carrier signal, in different multi-user scenarios.

that can be observed in Figure 5.26 are a combined result of the IF amplifier bandwidth, demodulator bandwidth and the non-linearity of the output buffer.

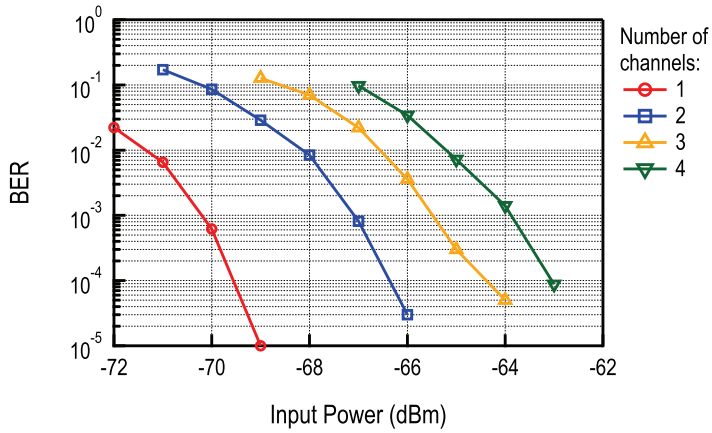
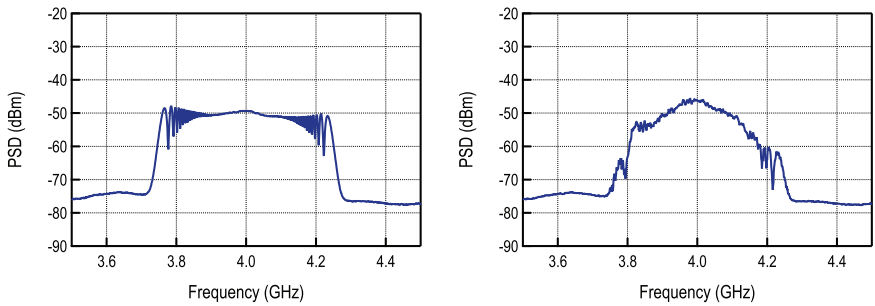



**Figure 5.27** BER curves for different number of broadcast sub-channels.

### 5.4.4 Multi-Channel Transmission Measurements

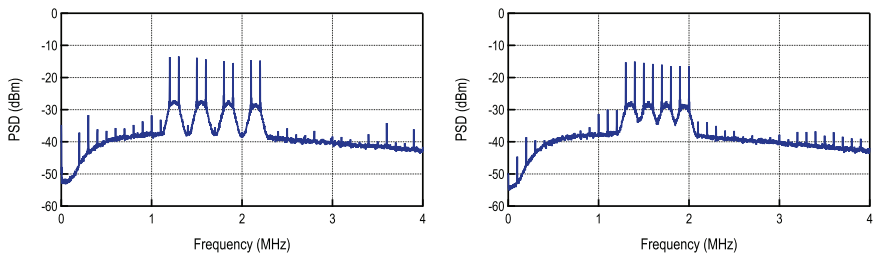
The multi-channel (MC) transmission concept was also tested with the implemented receiver. The BER curves for different number of sub-channels are shown in Figure 5.27. Compared to the case with multiple transmitters, a significant sensitivity loss can be observed. This is a consequence of scaling since the SNR of a single channel is proportional to $1/M^2$, where $M$ is the number of sub-channels. Nevertheless, for short range applications, where distance between nodes does not exceed several meters, such as BAN, the proposed scheme could still be used and could be of particular interest when a large number of nodes are present and need to receive different data simultaneously. The transmitted spectrum is compared in Figure 5.28 for the cases of a single FM-UWB signal and multiple sub-carrier FM-UWB signal. Since the modulating signal is no longer a triangular waveform, spectral flatness is lost.

One important difference between SC-FDMA with multiple transmitters and a single transmitter is that, in the latter, sub-channels are perfectly synchronized. For multiple transmitters, even if the orthogonal frequencies are used for different sub-channels, the orthogonality is preserved only if symbols are perfectly synchronized. Since it is practically impossible to synchronize multiple transmitters, sub-channels must be separated and a channel filter is required. In the case of a single transmitter, the sub-channels remain perfectly orthogonal, so there is no need for separation, and hence more channels can be placed in the same sub-carrier band. As long as the orthogonality is




(a) Standard FM-UWB spectrum (b) MC FM-UWB spectrum

**Figure 5.28** Spectrum of the transmitted signal, for the standard FM-UWB and MC FM-UWB.




(a) 100 kHz separation (b) No separation

**Figure 5.29** Demodulated signal spectrum, with and without spacing between adjacent sub-channels.

maintained, this separation will not influence the BER. In this regard, the proposed FDMA scheme is similar to the Orthogonal Frequency Division Multiplexing (OFDM) combined with the FM-UWB spread spectrum technique. The spectrum of the demodulated sub-carrier signal with and without separation is shown in Figure 5.29. Measured BER was not influenced by the channel separation.

## 5.5 Summary

The proposed receiver is compared to the State-of-the-Art receivers in Table 5.2. Of all the implemented FM-UWB receivers it consumes the lowest amount of power while still attaining sufficient sensitivity for short range communications in a HD-WSN. The delay-line demodulator based receivers from [12, 13] have an order of magnitude higher power consumption. The

**Table 5.2** Comparison with the state-of-the-art receivers

| Parameter | [13] | [12] | [18] | [19] | [17] | This Work |
|---|---|---|---|---|---|---|
| **SC-FDMA** | **Yes** | **Yes** | – | **No** | **No** | **Yes** |
| Demodulator | DL | DL | Regen. | Regen. | Regen. | DL |
| Frequency | 7.5 GHz | 4 GHz | 3.75 GHz | 8 GHz | 4 GHz | 4 GHz |
| **Power Conns.** | **9.1 mW** | **10 mW** | **3.8 mW** | **0.6 mW** | **580 $\mu$W** | **423 $\mu$W** |
| Supply | 1.8 V | 2.5 V | 1 V | 1 V | 1 V | 1 V |
| Max. Data Rate | 50 kb/s | 62.5 kb/s | 100 kb/s | 1 Mb/s | 100 kb/s | 400 kb/s |
| Sensitivity | −88 dBm | −46 dBm | −78 dBm | −76 dBm | −80.5 dBm | −70 dBm |
| Efficiency | **182 nJ/b** | **160 nJ/b** | **38 nJ/b** | **0.6 nJ/b** | **5.8 nJ/b** | **1.06 nJ/b** |
| Technology | 0.25 $\mu$m BiCMOS | 0.18 $\mu$m BiCMOS | 65 nm CMOS | 65 nm CMOS | 65 nm CMOS | 65 nm CMOS |

receiver in [17] achieves comparable consumption while providing better sensitivity. The low power consumption is obtained by using a narrow-band amplifier at the input. Since the demodulation is performed using a high-Q RF filter, with a very non-linear FM-AM conversion characteristic, it will not be possible to distinguish between different FM-UWB users. A modification of a regenerative receiver was proposed in [18] that uses two RF filter paths to achieve better linearity and loosen the Q constraints, but it consumes 3.8 mW. This receiver could potentially be utilized in a multi-user scenario; however, this capability was not demonstrated. The same receiver architecture was used to demodulate a Chirp-UWB signal in [19]. Even though the receiver consumes a peak power of 4 mW, the average power is decreased to 0.6 mW by employing duty cycling. The receiver proposed here already consumes low power in continuous operation, however, by applying the same duty-cycling technique, its power consumption could be reduced below 200 $\mu$W, which might be addressed in future research.

Aside from the low power achieved, the proposed receiver offers the capability for several FM-UWB users to communicate in the same RF band at the same time. In an environment where a lot of nodes need to operate in a small area, SC-FDMA can provide more flexibility for protocol optimization, and lead to lower latency by allowing multiple nodes to communicate at the same time. The only two other receiver implementations offering the same capability require an order of magnitude higher power, thus making the proposed receiver a better solution for the given scenario. In addition,

the implemented receiver could support different data rates and different M-FSK modulations. With a flexible digital baseband it would be possible to dynamically adjust the number of channels and data rate per channel, allowing to further optimize network performance.

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