Intelligent Edge-Embedded Technologies for Digitising Industry

RIVER PUBLISHERS SERIES IN COMMUNICATIONS AND NETWORKING

Series Editors

ABBAS JAMALIPOUR

The University of Sydney Australia

MARINA RUGGIERI

University of Rome Tor Vergata Italy

The "River Publishers Series in Communications and Networking" is a series of comprehensive academic and professional books which focus on communication and network systems. Topics range from the theory and use of systems involving all terminals, computers, and information processors to wired and wireless networks and network layouts, protocols, architectures, and implementations. Also covered are developments stemming from new market demands in systems, products, and technologies such as personal communications services, multimedia systems, enterprise networks, and optical communications.

The series includes research monographs, edited volumes, handbooks and textbooks, providing professionals, researchers, educators, and advanced students in the field with an invaluable insight into the latest research and developments.

Topics included in this series include:-

- Communication theory
- Multimedia systems
- Network architecture
- Optical communications
- Personal communication services
- Telecoms networks
- Wifi network protocols

For a list of other books in this series, visit www.riverpublishers.com

Intelligent Edge-Embedded Technologies for Digitising Industry

Editors

Ovidiu Vermesan

SINTEF, Norway

Mario Diaz Nava

STMicroelectronics, France



Published, sold and distributed by: River Publishers Alsbjergvej 10 9260 Gistrup Denmark

www.riverpublishers.com

ISBN: 978-87-7022-611-0 (Hardback) 978-87-7022-610-3 (Ebook)

©The Editor(s) (if applicable) and The Author(s) 2022. This book is published open access.

Open Access

This book is distributed under the terms of the Creative Commons Attribution-Non-Commercial 4.0 International License, CC-BY-NC 4.0) (http://creativecommons.org/licenses/by/4.0/), which permits use, duplication, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, a link is provided to the Creative Commons license and any changes made are indicated. The images or other third party material in this book are included in the work's Creative Commons license, unless indicated otherwise in the credit line; if such material is not included in the work's Creative Commons license and the respective action is not permitted by statutory regulation, users will need to obtain permission from the license holder to duplicate, adapt, or reproduce the material.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

The publisher, the authors and the editors are safe to assume that the advice and information in this book are believed to be true and accurate at the date of publication. Neither the publisher nor the authors or the editors give a warranty, express or implied, with respect to the material contained herein or for any errors or omissions that may have been made.

Printed on acid-free paper.

Dedication

"Wise thinkers prevail everywhere."

- Sophocles

"Intelligence is what you use when you don't know what to do."

- Jean Piaget

"The intelligence is proved not by ease of learning, but by understanding what we learn."

- Joseph Whitney

"A computer would deserve to be called intelligent if it could deceive a human into believing that it was human."

- Alan Turing

Acknowledgement

The editors would like to thank all the contributors for their support in the planning and preparation of this book. The recommendations and opinions expressed in the book are those of the editors, authors, and contributors and do not necessarily represent those of any organizations, employers, or companies.

Ovidiu Vermesan Mario Diaz Nava

Contents

Pı	reface			XV
Li	ist of l	Figures		xvii
Li	ist of T	Fables		xxiii
Li	ist of (Contrib	outors	xxv
Li	ist of A	Abbrevi	ations	xxix
1	Ope Ovid	rations liu Vern	AI Technologies for Next-Generation Autonomous with Sustainable Performance mesan, Frédéric Pétrot, Marcello Coppola,	1
			nneider, Alfred Höß	2
	1.1		rial AI	
		1.1.1	Challenges of Industrial AI versus Consumer AI	
	1.0	1.1.2		
	1.2	_	ilities Spectrum of Industrial AI	
	1.3		dustrial AI Spectrum	
		1.3.1	Narrow AI vs. General AI	
			Weak AI vs. Strong AI	
		1.3.3	1	13
		1.3.4	Red AI vs. Green AI	
	1.4	AI Pro	oblem Solving Domains	
		1.4.1	Expert Systems	14
		1.4.2	Machine Vision	17
		1.4.3	Robotics	18
		1.4.4	Biomimicry	20
		1.4.5	Genetic and Evolutionary Algorithms	22
		1.4.6	Generative AI	
		1.4.7	Artificial Swarm Intelligence	27

		1.4.8	Natural Language Processing	28
		1.4.9	Machine learning	29
		1.4.10	Neural Networks	30
		1.4.11	Automated Planning and Plan Recognition	32
		1.4.12	AI for the Metaverse	34
	1.5	Edge A	AI continuum	34
	1.6		olic AI – ML Continuum	38
	1.7	Logic-	based AI: Knowledge Representation and Reasoning.	39
	1.8	Hardw	are/Software Technology Stack	42
		1.8.1	ML Methods and Techniques	44
		1.8.2	Neural Networks Architectures	50
		1.8.3	Industrial Embedded AI/ML	52
		1.8.4	On-device ML Applications Enabling True Edge	
			Computing	55
		1.8.5	Machine Learning on Embedded Devices	57
		1.8.6	Embedded ML Development Flow in Industrial	
			Setting	6
	1.9	Summa	ary	67
		Refere	nces	69
_		_		
2			and Hardware for Neuromorphic Computing	73
2	Björ	n Debai	llie, Ilja Ocket, and Peter Debacker	
2	<i>Björ</i> 2.1	n Debai Mobile	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing	74
2	<i>Björ</i> 2.1 2.2	n <i>Debai</i> Mobile Neuror	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI	74 74
2	<i>Björ</i> 2.1	n Debai Mobile Neuror Buildir	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	73 74 74 76
2	<i>Björ</i> 2.1 2.2	m Debail Mobile Neuror Buildir 2.3.1	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76
2	<i>Björ</i> 2.1 2.2	n Debai Mobile Neuror Buildir	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76 77
2	<i>Björ</i> 2.1 2.2	n Debai. Mobile Neuror Buildir 2.3.1 2.3.2	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76 77
2	<i>Björ</i> 2.1 2.2	m Debail Mobile Neuror Buildir 2.3.1	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76 73
2	Björ 2.1 2.2 2.3	n Debai. Mobile Neuror Buildir 2.3.1 2.3.2	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76 73 78
2	Björ 2.1 2.2 2.3	n Debai. Mobile Neuror Buildir 2.3.1 2.3.2 2.3.3 Positio	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76 75 78 78
2	Björ 2.1 2.2 2.3	n Debai. Mobile Neuror Buildir 2.3.1 2.3.2 2.3.3 Positio Targete	Ellie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI	74 74 76 75 78 78 78 81
2	Björ 2.1 2.2 2.3	n Debai. Mobile Neuror Buildir 2.3.1 2.3.2 2.3.3 Positio Targete 2.5.1	Ellie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76 75 78 78 78 81
2	Björ 2.1 2.2 2.3	n Debai. Mobile Neuror Buildir 2.3.1 2.3.2 2.3.3 Positio Targete	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76 77 78 78 78 81 82
2	Björ 2.1 2.2 2.3	n Debai. Mobile Neuror Buildir 2.3.1 2.3.2 2.3.3 Positio Targete 2.5.1 2.5.2	llie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76
2	Björ 2.1 2.2 2.3	n Debai. Mobile Neuror Buildir 2.3.1 2.3.2 2.3.3 Positio Targete 2.5.1	Ellie, Ilja Ocket, and Peter Debacker E Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI Ing Neuromorphic Hardware	74 74 76 76 78 78 78 81 82 82
2	Björ 2.1 2.2 2.3	m Debai. Mobile Neuror Buildir 2.3.1 2.3.2 2.3.3 Positio Targete 2.5.1 2.5.2 2.5.3	Ellie, Ilja Ocket, and Peter Debacker Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI ng Neuromorphic Hardware	74 74 76 77 78 78 79 81 82
2	Björ 2.1 2.2 2.3	n Debai. Mobile Neuror Buildir 2.3.1 2.3.2 2.3.3 Positio Targete 2.5.1 2.5.2	Ellie, Ilja Ocket, and Peter Debacker E Devices Call for Efficient Neuromorphic Computing morphic Hardware Enables Next Generation AI Ing Neuromorphic Hardware	74 74 76 76 78 78 78 81 82 82

				Conte	nts ix
	2.6 2.7	Conclu	morphic H usion	Health – Medical Image Denoising ardware Technologies Being Developed	. 84 . 86
3	a Ne	eural No	etwork on	gies for Training, Profiling, and Mapping a Hardware Target imon Narduzzi, Muhammad Arsalan,	89
	Kay	Bierzyn	ski, Stefan	o Traferro, Preetha Vijayan,	
				Manolis Sifalakis, Rene Van Leuken,	
	•		Rashid A Diaz Nava	li Maen Mallah, Bijoy Kundu, Loreto Mat	еи,
	3.1		uction		. 90
	3.1	3.1.1		mputing Benefices and Challenges	
		3.1.2	Artificial	Neural Networks (ANNs) and Spiking	
		~		etworks (SNNs)	
	3.2			f key aspects of Neural Networks	
		3.2.1		SNN Hardware Aware Design	
		3.2.2		ONN C	
		3.2.3		SNN Conversion	
		3.2.4		e Gradient Descent	
	2.2	3.2.5		ngineering Object (Nengo) Simulator	
	3.3	3.3.1		on: Temporal Delta Layer	
		3.3.1	_	l Delta Layer: Training Towards Brain Temporal Sparsity for Energy Efficient Deep	
				etworks	
		3.3.2		Works	
		3.3.3		logy	
		3.3.3	3.3.3.1	Delta inference	
			3.3.3.2	Activation quantization to induce sparsity	
			3.3.3.3	Fixed point quantization	
			3.3.3.4	Learned step-size quantization	
			3.3.3.5	Sparsity penalty	
			3.3.3.6	Proposed algorithms	. 110
		3.3.4		ents and Results	
			3.3.4.1	Baseline	
			3.3.4.2	Experiments	
			3.3.4.3	Accuracy v/s Activation sparsity	. 113
	3.4	NN Co	ompiler for	Dedicated Inference Accelerator Hardware	

x Contents

		3.4.1	Compiler Components	116
		3.4.2	ONNX Parser	117
		3.4.3	Hardware Architecture Representation	118
		3.4.4	Mapper	119
		3.4.5		120
		3.4.6	Mapping of Deep Spiking NN Architectures	
			to Digital SNN Inference Devices	121
	3.5	Simula		123
	3.6			127
		3.6.1		127
		3.6.2	On NN Compiler for Dedicated Inference	
			Accelerator Hardware with Analog In-Memory	
				128
		3.6.3		128
		Refere		129
4	Usir	ıg FeFE	ETs as Resistive Synapses in Crossbar-based Analog	
	MA	C Accel	lerating Units	137
	Lei Z	Zhang, 1	David Borggreve, Frank Vanselow, Ralf Brederlow	
	4.1	Introd	uction and Background	138
	4.2	Requir	rements of Crossbar Structure on eNVMs	139
	4.3	Synap	8	144
		4.3.1		144
		4.3.2	Gate-Cascaded FeFETs	146
		4.3.3	Exploration Results	148
	4.4	Conclu	usion	150
		Refere	ences	151
5			v 1 8	153
			ii, Taha Soliman, Alptekin Vardar,	
			s Kämpfe	
	5.1		•	154
	5.2		,	154
		5.2.1		154
		5.2.2		155
		5.2.3	1	156
			\mathcal{E}	156
			C 11	159
		5.2.4	Target Network Quantization	160

			Contents	XI
		5.2.4.1 Floating point architectures		160
		5.2.4.2 Fixed-point architectures		161
		5.2.4.3 Binarized architectures		161
		5.2.4.4 Flexible precision architectures		161
		References		162
6		ficial Intelligence Advancements for Digitising Indus	stry	167
		diu Vermesan, and Reiner John		1.00
	6.1	AI at the Edge in Industrial Processes		168
	6.2	A pan-European AI Framework for Manufacturing		170
	()	and Process Technology		170
	6.3 6.4	AI Technologies		180 182
	0.4	AI Application Areas		
		6.4.1 Automotive		183 185
				186
		3		188
				190
	6.5	6.4.5 Transportation		190
	6.6	Conclusion		192
	0.0	References		193
7	Imp	act of AI and Digital Twins on HoT		195
	_	Han, Björn Richerzhagen, Hans Schotten, Davide Calar	ndra,	
		Fabrizio Lamberti	ŕ	
	7.1	Introduction to the Hexa-X Project		195
	7.2	An Ecosystem Concept for Digital Twins in IIoT		196
	7.3	Digital Twins for Emergent Intelligence		197
	7.4	Network-aware Digital Twins for Local Insight Gener	ation .	200
	7.5	AI at the Intersection between DTs and HMI in Indust	rial	
		IoT		201
	7.6	Conclusion		203
		References		203
8		son Learnt and Future of AI Applied to Manufacturi	ing	207
		rio Frascolla, Matthias Hummert, Tobias Monsees,		
		: Wübben, Armin Dekorsy, Nicola Michailow, Volkmar	Döricht,	
		istoph Niedermeier, Joachim Kaiser, Arne Bröring,		
	Micl	hael Villnow, Daniel Wessel, Florian Geiser, Matthia	s Wissel,	

	Albe	rto Vise	eras, Bin Han, Björn Richerzhagen, Hans Schotter	ı,
	Davi	ide Cala	ndra, and Fabrizio Lamberti	
	8.1	Introdu	action	208
	8.2	IoT En	abled by Machine Learning	209
	8.3		ne Learning at the Edge	210
		8.3.1	Applications of $EdgeML$ in Industrial IoT	211
		8.3.2	Challenges in $EdgeML$	212
	8.4	Federa	ted Learning – A Solution to Train ML Models	213
		8.4.1	Applications for Federated Learning in Industrial	
			IoT	214
		8.4.2	Federated Learning Scenarios	215
		8.4.3	Challenges in Federated Learning	217
		8.4.4	Frameworks and products for leveraging Federated	
			Learning	218
		8.4.5	Reducing Complexity of RX Processing	220
		8.4.6	Enhancing Reliability by Multi-Connectivity in the	
			Uplink	223
	8.5	Comm	unications in an "Embodied Artificial Intelligence"	
				227
	8.6		lied Artificial Intelligence	228
	8.7		ntegration as a Central Technological Driver	230
	8.8		sion	233
		Referei	nces	233
9	Ethi	cal Can	siderations and Trustworthy Industrial AI Systems	241
,			esan, Cristina De Luca, Reiner John,	4 41
			ppola, Björn Debaillie, and Giulio Urlini	
	9.1		action	242
	9.2		and Responsible AI in Industrial Environments	245
	9.3		ements for Industry-Grade AI	246
	9.4		ial AI Challenges	250
	,,,	9.4.1	Complexity	251
		9.4.2	Use of Natural Resources	251
		9.4.3	Pollution and Waste	252
		9.4.4	Energy	252
	9.5	Ethical	Considerations for Digitising Industry	253
		9.5.1	AI Trustworthiness	253
		/ · · · · ·	Al Hustworthiness	20.
		9.5.2	Bias and Fairness	254

				Contents	xiii
		9.5.4	Accountability		255
		9.5.5	Explainability		256
		9.5.6	Control		257
		9.5.7	Human-Machine Interaction and Manipulation		
			of Behaviour		257
		9.5.8	Autonomous Industrial Systems		258
		9.5.9	Machine Ethics		260
		9.5.10	Automation and Employment		260
	9.6		the Future Digitising Industry		261
	9.7		Guidelines for AI in Industrial Environments		262
	9.8	Recom	mendations for Ethical AI in Industrial		
		Enviro	nments		262
	9.9	Conclu	sion		265
		Referei	nces		266
10			allenges of AI Standardisation in the D	igitising	
	Indu	•			271
			esan, Marcello Coppola, Reiner John,		
			Luca, Roy Bahr, and Giulio Urlini		
			ction		272
			tional Principles		273
			AI Standardisation in Digitising Industry .		274
	10.4		nges Associated with AI Deployments in In		
			nments		275
			ndardisation Needs in Industrial Automation		276
			rdisation of Security and Safety in AI System		278
	10.7		lobal AI Standards Landscape and Standards		
		Activiti			280
			CEN-CENELEC		282
			ETSI		282
			IEC		283
			<u>ISO</u>		284
		10.7.5			288
		10.7.6			289
	10-		ITU-T		290
			tification		291
			mendations for an AI Standardisation Roadm	•	293
	10.10		usion		296
		Refere	ences		297

xiv Contents

Index	301
About the Editors	307

Preface

Intelligent Edge-Embedded Technologies for Digitising Industry

Industrial intelligent edge systems are designed with more computing power and sensors to enable analytics, AI inferencing, and natural user interfaces. These new capabilities enhance their behaviour and provide new functionalities based on sensing, actuating, programming, and connectivity to dynamically interact and autonomously function.

Intelligent edge architectures are complementary to embedded systems, bringing scalable computing nearer to resource-constrained embedded systems and enabling these systems to leverage more complex, computing-intensive processes (including machine and deep learning) and local processing of historical data.

Intelligent edge devices are often resource-constrained by design. Such fixed-function systems are highly optimised for performance (speed, reliability, safety) and cost.

By making additional computing resources available to these systems, intelligent edge deployments enable diverse decision-making processes in the local industrial environment. These include system-level optimisations across devices, changes to the programming of specific devices, and other forms of control.

AI algorithms are processed locally, directly on the device, on the gateway, or on-premises servers near the edge devices. The algorithms utilise the data generated by the devices themselves. Industrial edge IIoT devices can make independent decisions in a matter of milliseconds without having to connect to the cloud.

As the computing and microcontroller architectures evolve, they support edge AI on embedded industrial systems and make the most of the limited computing resources there. The ARM Cortex cores, and AI accelerator's developments are pushing forward AI in resource-constrained environments. Several chip manufacturers are directly enabling machine learning-based AI on their microcontrollers. The increased hardware support for AI, including

xvi Preface

tools for edge AI, opens new opportunities for industrial edge AI implementations and deployments with new AI configurations that can operate in real-time and be integrated into the industrial manufacturing process.

This book provides a valuable resource for researchers working with intelligent edge-embedded technologies for digitising industry and industry professionals, machine and deep learning engineers, front-end developers, IIoT developers, and back-end developers looking to deploy intelligent solutions at the industrial edge.

List of Figures

Figure 1.1	AI systems capabilities	9
Figure 1.2	Narrow AI vs General AI	12
Figure 1.3	AI problem solving domains	15
Figure 1.4	Typical expert system architecture	15
Figure 1.5	Typical CNN-based machine (left) and workflow	
	(right)	18
Figure 1.6	Self-driving vehicles: Training and inference	
	(generate steering commands)	19
Figure 1.7	Life's principles	21
Figure 1.8	Using Genetic Algorithms in the iterative process of	
	fine-tuning NN hyperparameters	24
Figure 1.9	Discriminative (left) vs Generative (right) Models	
	in ML	25
Figure 1.10	Network architecture of generator and discriminator	
	based on deep convolutional GAN	26
Figure 1.11	Swarm intelligence visualized: population of agents	
	searching for a destination (left) and search space	
	represented by a nonlinear regression generated	
	surface (right)	28
Figure 1.12	Perceptron illustration	31
Figure 1.13	Automated planning, states, and actions	32
Figure 1.14	Application of Metaverse	34
Figure 1.15	AI across the edge continuum	36
Figure 1.16	Knowledge representation	40
Figure 1.17	Type of knowledge	41
Figure 1.18	Five-layer (with sublayers) AI technology stack	43
Figure 1.19	ML taxonomy	45
Figure 1.20	Regression visualized 2D (left), 3D (right)	45
Figure 1.21	Normal(blue) - abnormal(red) (left). Predicted	
	values using logistic regression (right)	46
Figure 1.22	Classification (left) vs Regression (right)	47

Figure 1.23	Cluster (Gaussian mix) 4 clusters (left) vs 2 clusters	
	(right)	48
Figure 1.24	Principal component analysis. Intuitive visualisa-	
	tion, select variables that capture the largest	
	variability in data	48
Figure 1.25	Q-Learning vs Deep Q-Learning	49
Figure 1.26	Typical CNN architecture	51
Figure 1.27	The repeating module underlying RNN	
J	architecture	52
Figure 1.28	Example of an architecture useful for fault diagnosis.	52
Figure 1.29	Embedded ML design and development ecosystem	
O	view	55
Figure 1.30	Embedded ML optimisation	58
Figure 1.31	ML hardware options for various AI tasks	59
Figure 1.32	Comparison of the von Neumann architecture with	
O	the neuromorphic architecture	61
Figure 1.33	The high-level embedded ML development flow	62
Figure 1.34	Temporal and frequency plots as input to motor	
O	classification	63
Figure 1.35	Hyperparameters (outside the model) vs parameters	
O	(inside the model)	64
Figure 1.36	Categories of datasets and where they are used	64
Figure 1.37	Confusion matrix	66
Figure 2.1	TEMPO spreads over three action areas	76
Figure 2.2	TEMPO positioned in the greater landscape of	
J	neuromorphic computing	80
Figure 2.3	Possible inputs for the western food classification	
_	DNN	83
Figure 2.4	3D landscape, ordering of 3D technologies	
J	according to the system-level wiring hierarchy	85
Figure 3.1	Networks to hardware workflow	95
Figure 3.2	Spiking neuron models	99
Figure 3.3	(a) Standard DNN and (b) DNN with temporal delta	
-	layer	101
Figure 3.4	Sparsity in Δx can save multiplications between Δx	
-	and columns of W that correspond to zero	103
Figure 3.5	Demonstration of two consecutive activation maps	
_	leading to near zero deltas	106

Figure 3.6	Importance of step size in quantization: on the right side, in all three cases, the data is quantized to five bins with different uniform step sizes, but without	
F: 25	optimum step size value, the quantization can alter the range and resolution of the original.	108
Figure 3.7	Methodology flow of temporal delta layer with fixed point quantization.	111
Figure 3.8	Methodology flow of temporal delta layer with	111
118	learned step size quantization	112
Figure 3.9	Evolution of step size from initialization	
_	to convergence. As step-size is a learnable param-	
	eter, it gets re-adjusted during training to cause	
	minimum information loss in each layer	115
Figure 3.10	Overview of Compiler Tool	117
Figure 3.11	ONNX Parser diagram of parsing and fusing the	
	input ONNX model into a list of Nodes and Fused	
	Nodes	118
Figure 3.12	Mapping flow of the Compiler	119
Figure 3.13	Mapping of layers 1 and 2 on processing core 1	121
Figure 3.14	A HW architecture for SNN inference	122
Figure 3.15	An example of a deep spiking network that will be	400
F: 246	mapped to a HW architecture	123
Figure 3.16	MobileNet V1 parameters per layer	124
Figure 3.17	MobileNet V1 data volume per layer, normalized to	104
E: 2 10	input data volume.	124
Figure 3.18	MobileNet V1 bandwidth (Gb/s) at each layer	125 126
Figure 3.19 Figure 3.20	N2D2: Neural Network Design & Deployment Process flow: (a,b) conversion of the neural network	120
rigure 3.20	to the hardware representation, (c) tuning of the	
	layer parallelism at architectural level, (d) tuning of	
	the buffer, (e) post-processing	126
Figure 4.1	(a) shows FeFETs' abstract structure, where	120
1 iguit 4.1	a ferroelectric layer is placed at the top of the	
	transistor's gate. The threshold voltage of FeFETs	
	can be programmed by adapting the polarity of	
	the ferroelectric layer and coded as shown in (b).	
	(c) illustrates possible cumulative distribution func-	
	tions (CDFs) of real FeFET's current in High-/Low-	
	V _{TH} states, where a state-overlap happens, and the	
	operating window vanishes	139

Figure 4.2	Implementations of analogue MAC accelerating	
	units using single-ended (a) and pseudo-differential	
	(b) structures are shown	140
Figure 4.3	The numerical analysis indicates that the $R_{\rm OFF}/R_{\rm ON}$	
	plays a dominant role for the computation precision	
	in the single-ended structure, where the inherent	
	device process variation is more important for the	
	pseudo-differential structure	143
Figure 4.4	Two conventional FeFET synapses are shown,	
	where synapse (b) has an additional current-limiting	
	resistor in the series connection compared to the	
	stand-alone FeFET synapse (a). Both synapses can	
	be activated by connecting a certain gate-voltage	
	using access transistors $M_{\rm a}$ and $M_{\rm b}$, respectively.	
	(c) shows the characteristics of synapses (a) and (b),	
	where a large series resistor enlarges the threshold	
	voltage range of individual states by scarifying the	
	number of available states	144
Figure 4.5	The proposed gate-cascaded FeFET synapse, where	
	a diode-connecting FeFET is connected to the gate	
	of another FeFET, is shown in (a). Its statistical dis-	
	tribution is shown in (b), that the distance between	
	threshold voltages doubles and the variation of the	
T1 4 6	state overlap.	146
Figure 4.6	(a) and (b) show a two-stage and a N-stage gate-	
	cascaded FeFET synapse, respectively. (c) shows	
	the change of their characteristics, where the volt-	
	age difference between states is enlarged. (d)	
	demonstrate the characteristic of a conventional	
	synapse with three serially connected FeFET and	
	a three-stage gate cascaded FeFET. The gate-	
	cascaded FeFET achieved 12.1 times larger oper-	1.40
E: 4.7	ating window than conventional design	149
Figure 4.7	design example, which combine the proposed and	
	conventional techniques, is shown in (a). (b) dis-	
	plays the layout of this design example. (c) indicates	
	that a up to 200mV operating window is achieved	150
	using 1-stage gate-cascade	150

Figure 5.1	Conventional volatile memory cells a) 6T SRAM	154
Figure 5.2	cell and b) DRAM cell	154 157
Figure 5.3	Eliminated the DACs and instead serialize the activation by applying only a single bit at each cycle	158
Figure 5.4	(a) Several row activation approach such as Ambit's TRA. (b) Changing subarray unit cell structure whether with extra transistors or operation mode as in DRISA 3T1C. (c) Activating only one row at a time and use the row activation as an operand as in	136
Figure 5.5	FlexPim	159
Figure 5.5	The relation between the energy cost for digital and analog MAC operations versus bit precision	160
Figure 6.1	AI4DI Objectives	172
Figure 6.2	AI4DI Key Targets	173
Figure 6.3	Silicon-born AI effect on Moore's Law beyond the	
Figure 7.1	current silicon technology developments The ecosystem of 6G human-centric industrial DTs, with the arrows indicating the direction of the	180
	information flow.	197
Figure 7.2	Comparing the conventional AI solutions based on centralized AI (left) and FL (middle) to EI (right).	198
Figure 7.3	Illustration of collaborating DTs in IIoT	201
Figure 8.1	The global model is first trained in a central location	201
rigure o.r	and then broadcast to edge devices for inference.	
	Edge devices can return data samples to train and	
	update the global model	213
Figure 8.2	Visualization of the FL process. The four steps are	41 J
1 iguit 0.2	executed consecutively and are repeated following	
	the same process until the global model converges.	214

xxii List of Figures

Figure 8.3	FL scenarios according to how the data is split	
	across clients. (a) Horizontal FL. (b) Vertical FL	216
Figure 8.4	Efficiency η over SNR for standard ARQ scheme	
	in comparison to E-ARQ with NN-FoC forecasting	
	and a Genie forecaster for different decoder	
	delays κ	222
Figure 8.5	Distributed communication system with J access	
_	points forwarding compressed messages to the DU.	224
Figure 8.6	BER performance for 16-QAM with RAPs apply-	
J	ing SNR-adapted 6-bit quantizer per AP and REMC	
	in DU for $\mathbf{J} \geq 1$	226
Figure 8.7	The cognitive cycle of an embodied intelligence	
	agent	229
Figure 8.8	Overview of mmW frequencies. 5G bands expand	
	up to 50 GHz, 6G is expected to reach 1 THz and	
	also include visible light communications	231
Figure 8.9	Overview of the functions of mmW wireless tech-	
	nology.	232
Figure 9.1	A framework for trustworthy industrial AI systems.	245
Figure 9.2	Complexity of applicability of ethical considera-	
	tions resulting from the interaction of subsystems	247
Figure 9.3	Requirements for industry-grade AI	247
Figure 9.4	Reference architecture for AI-based autonomous	
	systems in industrial environments	259
Figure 10.1	NIST focus areas for standards development	273
Figure 10.2	Three-layer AI topics structure: generic, horizontal,	
	and relevant industrial application areas	277
Figure 10.3	Industrial AI standards system framework	281
Figure 10.4	Classification scheme along with criticality, AI	
	methods and capabilities	293

List of Tables

Table 2.1	Edge AI use cases addresses in TEMPO covers five	
	application domains	82
Table 3.1	Spatial stream - comparison of accuracy and activation sparsity obtained through the proposed scenarios against the benchmark. In the case of fixed-point quantization, the reported results are for a bit width of	110
T. 1.1. 2.2	6 bits	113
Table 3.2	Temporal stream - comparison of accuracy and activation sparsity obtained through the proposed scenarios	
	against the benchmark. In the case of fixed-point quan-	
	tization, the reported results are for a bit-width of	
	7 bits	114
Table 3.3	Result of decreasing activation bit-width to increase	
	activation sparsity while maintaining accuracy. For	
	spatial stream, decreasing below 6 bits caused the	
	accuracy to drop considerably. For temporal stream,	
	the same happened below 7 bits	114
Table 3.4	Final results on 2 stream networks after average fus-	
	ing the spatial and temporal stream weights. With 5%	
	accuracy loss, the proposed method almost doubles the	
	activation sparsity available in comparison to the	
	baseline	127
Table 4.1	Comparison between single-ended and pseudo-	
	differential structures	144
Table 4.2	Relative Performance Comparison	148

List of Contributors

Ali, Rashid, Fraunhofer IIS, Germany

Arsalan, Muhammad, *Infineon, Germany*

Bahr, Roy, SINTEF AS, Norway

Bierzynski, Kay, Infineon, Germany

Borggreve, David, Fraunhofer EMFT, Germany

Bröring, Arne, Siemens AG, Germany

Brederlow, Ralf, Technical University of Munich, Germany

Calandra, Davide, Politecnico di Torino, Italy

Coppola, Marcello, STMicroelectronics, France

Döricht, Volkmar, Siemens AG, Germany

De Luca, Cristina, Silicon Austria Labs GmbH, Austria

Debacker, Peter, imec, Belgium

Debaillie, Björn, IMEC, Belgium

Dekorsy, Armin, University of Bremen, Germany

Frascolla, Valerio, Intel Deutschland GmbH, Germany

Geiser, Florian, Motius GmbH, Germany

Höß, Alfred, Ostbayerische Technische Hochschule Amberg-Weiden, Germany

Han, Bin, Technische UniversitÄd't Kaiserslautern, Germany

Hummert, Matthias, *University of Bremen, Germany*

John, Reiner, AVL List GmbH, Austria

Kämpfe, Thomas, Fraunhofer IPMS

xxvi List of Contributors

Kaiser, Joachim, Siemens AG, Germany

Kundu, Bijoy, Fraunhofer IIS, Germany

Laleni, Nellie, Fraunhofer IPMS

Lamberti, Fabrizio, Politecnico di Torino, Italy

Maen, Mallah, Fraunhofer IIS, Germany

Mateu, Loreto, Fraunhofer IIS, Germany

Michailow, Nicola, Siemens AG, Germany

Monsees, Tobias, University of Bremen, Germany

Muir, Dylan, SynSense, Switzerland

Narduzzi, Simon, CSEM, Switzerland

Nava, Mario Diaz, STMicroelectronics, France

Niedermeier, Christoph, Siemens AG, Germany

Ocket, Ilja, imec, Belgium

Pétrot, Frédéric, University Grenoble Alpes, CNRS, Grenoble INP, TIMA, France

Richerzhagen, Björn, Siemens Technology, Germany

Schneider, Mathias, Ostbayerische Technische Hochschule Amberg-Weiden, Germany

Schotten, Hans, Technische UniversitÄd't Kaiserslautern, Germany

Sifalakis, Manolis, Imec, The Netherlands

Soliman, Taha, Robert Bosch GmbH

Traferro, Stefano, Imec, The Netherlands

Urlini, Giulio, STMicroelectronics, Italy

Valentian, Alexandre, CEA, France

Van Leuken, Rene, TU Delft, The Netherlands

Vanselow, Fank, Fraunhofer EMFT, Germany

Vardar, Alptekin, Fraunhofer IPMS

Vermesan, Ovidiu, SINTEF AS, Norway

Vijayan, Preetha, Imec, The Netherlands

Villnow, Michael, Siemens AG, Germany

Viseras, Alberto, Motius GmbH, Germany

Wübben, Dirk, University of Bremen, Germany

Wessel, Daniel, Motius GmbH, Germany

Wissel, Matthias, Motius GmbH, Germany

Yousefzadeh, Amirreza, Imec, The Netherlands

Zhang, Lei, Fraunhofer EMFT, Germany; Technical University of Munich, Germany

List of Abbreviations

AP Access point

ARQ Automatic repeat request

ASIC Application specific integrated circuit

CPU Central processing unit

CU Central unit DL Deep learning

DSO Distribution system operator

DU Distributed unit
DT Digital twin
e2e End to end

FEC Forward error correction

FH Fronthaul

FL Federated learning

FPGA Field-programmable gate array GPU Graphic processing units

HW Hardware

IBM Information bottleneck method IIoT Industrial internet of things

IoT Internet of things
LUT Look-up-table
MedTech Medical technology

MIMO Multi-input multiple-output

ML Machine learning
NN Neural network
QA Quality assurance
RAN Radio access network

RU Radio unit

SDK Software development kit

SotA State of the art

SW Software

TSO Transmission system operator