A Novel Design of Low Power and High Speed 1-Bit and 4-Bit Magnitude Comparator

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Abstract

In order to boost speed, reduce space for compactness, and minimise power consumption, numerous innovative circuit designs must be developed. Comparators are a fundamental design module that can be used in VLSI, digital signal processors, and data processing application-specific integrated circuits. In this research, we suggested four distinct models of one-bit comparators and used model-4 to develop a four-bit comparator. The performance of these four different comparators was compared to that of an existing comparator, and it was determined that the proposed model 4 outperforms the existing comparator in terms of speed, power consumption, and area. The DSCH-3.1 software programme is used to develop and simulate the schematics. Then, using Microwind 3.1 software, they simulated Verilog files and examined the performance of different design comparators at 90nm and 120nm technologies. From the results we can conclude that designing a magnitude comparator using proposed model 4 design style we can reduce all parameters of transistor count, logic gates count, power consumption and delay by 30%, 40%, 58.38%, 38.688 % respectively for 1 bit comparator and 19.5%, 14.05%, 13.21%, 28.088% respectively for four-bit comparator.

Keywords. Magnitude Comparator, Area, Power Consumption, Delay, VerilogHDL

1. INTRODUCTION

The magnitude of two binary values, say X and Y, is compared using a digital magnitude comparator, which is a logic circuit. As depicted in Figure 1, the logic circuit will have three outputs that indicate if XY, X=Y, or X>Y is true. Table-1 depicts the truth table.

Conventional comparator consumes more area and delay due to it requires more transistors in CMOS design. In CMOS AND gate itself requires 6 MOS transistors and NOR requires 4 MOS transistors. Conventional one magnitude comparator requires 2 NOT, 2 AND and 1 NOR gate shown in Figure 2. All it takes 20 MOS transistors to implement in CMOS design. In a 4-bit magnitude comparator shown in Figure 3 have two binary numbers in which each of the binary number consists of four bits. The logic circuit of Four Bit Comparator consists of 8 NOT gates, 23 two input AND gates and 6 two input OR gates4 two input NOR gates. Here also we have three outputs X<Y, X=Y and X>Y. It requires 178 MOS transistors to implement in CMOS [1- 2].

Previously described works have been focused on designing comparator in transistor level using different design techniques. In this paper comparator is designed using 2 NOR gates and 1 XNOR gate where it requires only 14 MOS transistors to implement it in CMOS. This makes circuit simple, less area, low power and less delay. Using proposed model 4 designed four-bit comparator then simulated and compared results with existing comparator in both 90nm and 120nm technologies [3- 4].

The paper is organized as follows. The section 2 clearly explained different models of one bit magnitude comparator. This section clearly explains the designing of all four proposed models 1, 2, 3 and 4 and redundant Boolean expressions for every model and their logic diagrams. Simulation results of one bit and four-bit existing magnitude comparator and proposed model-4 comparator in 90nm and 120nm technologies are analyzed and discussed in Section 3. And finally, Section 4 concludes that designing a magnitude comparator using proposed model-4 have better performances than existing magnitude comparator.

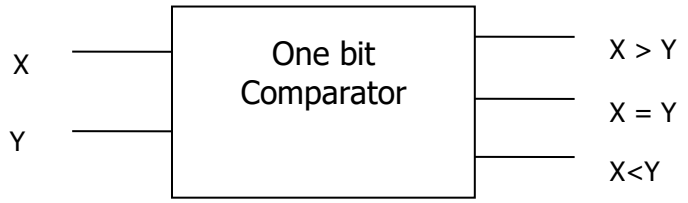

Figure 1. Block of one-bit Magnitude Comparator

Table1: Truth Table of one- Bit Magnitude Comparator

Input		**Output**		
X	Y	F (X>Y)	F (X=Y)	F (X<Y)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

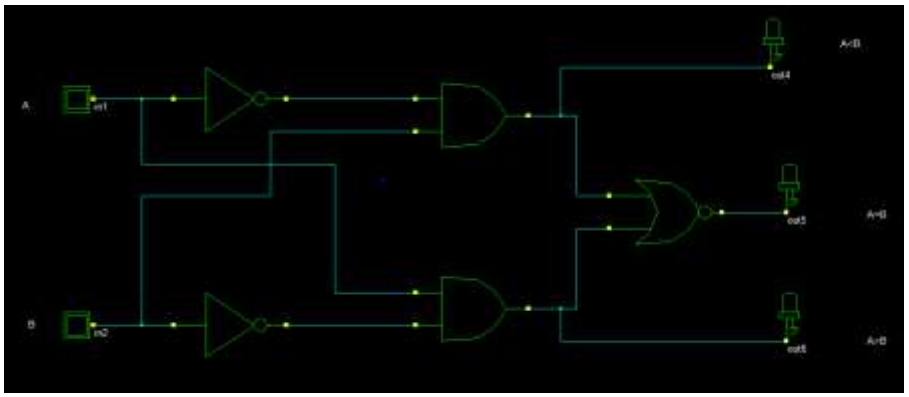

Figure 2. Implementation of existing one-bit Magnitude comparator

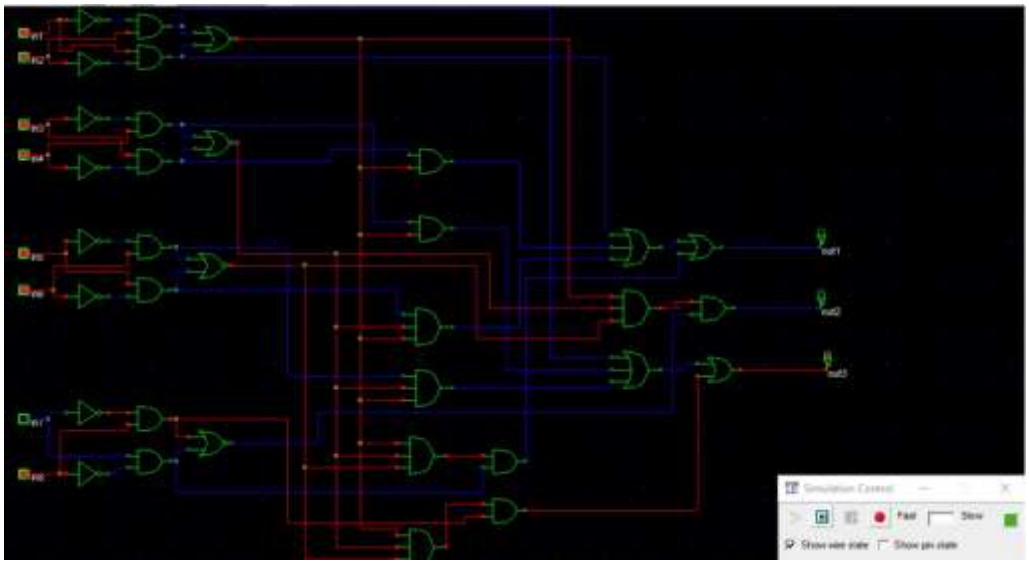

Figure 3. Implementation of existing 4-bit Magnitude comparator

2. PROPOSED MODELS

The proposed models are designed in terms of logic gates. The first two proposed models are designed using half subtractor logic. The proposed model 3 is modified version of proposed model 2 where it reduces one gate compare to proposed model 2 and also with existing comparator. Proposed model 4 is designed only using one XNOR and two NOR gates, this model requires only 3 gates and this model have better performance interms of area, power, delay when compared with existing comparator and also all proposed models [5- 6].

2.1. Proposed Model -1

As said above this model is designed by using half subtractor logic. The truth table in Table-2 shows that borrow of half subtractor is high if and only if the input Y is greater than X. And also, the Difference of half subtractor is low if and only if the both inputs are similar. The compliment of difference output of half subtractor gives X equals to Y output. The outputs Difference and Borrow of half subtractor fed to XOR gate to get X greater than Y [7- 9].

By adding one XOR and one NOT gate to half subtractor one bit magnitude comparator is realized in proposed model-1 as shown in Figure 4.The logical expressions for every output is realized below. The difference output of Half Subtractor is given to a NOT gate to get X equals to Y. Difference and Borrow is given to a XOR gate to get X Greater than Y. And Borrow of Half Subtractor equals to X Less than Y. This Proposed model 1 needs 2 XOR gates, 2 NOT gates and 1 AND gate [9- 11].

Table2: Truth Table of Half Subtractor

Input		Output	
X	Y	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

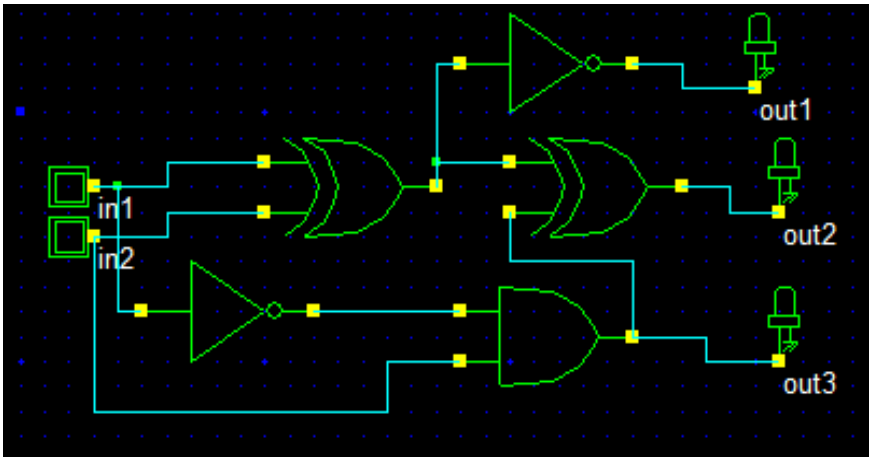

Figure 4. Implementation of Proposed-1one-bit Magnitude comparator

$$X<Y = \overline{X}Y$$

$$X = Y = \overline{\overline{X}Y + X\overline{Y}}$$

$$= \overline{\overline{X}Y}.\overline{X\overline{Y}}$$

$$= (X+\overline{Y})(\overline{X}+Y)$$

$$= XY + \overline{X}\overline{Y}$$

$$X > Y = (\overline{X}Y + X\overline{Y})\square\ (\overline{X}Y)$$

$$= (\overline{\overline{X}Y + X\overline{Y}}\ .X\overline{Y} + \overline{X\overline{Y}}\ )(\overline{X}Y + X\overline{Y})$$

$$= (XY+\overline{X}\overline{Y})X\overline{Y} + (X+\overline{Y})(\overline{X}Y + X\overline{Y}\ )$$

$$= X\overline{Y}$$

2.2. Proposed Model-2

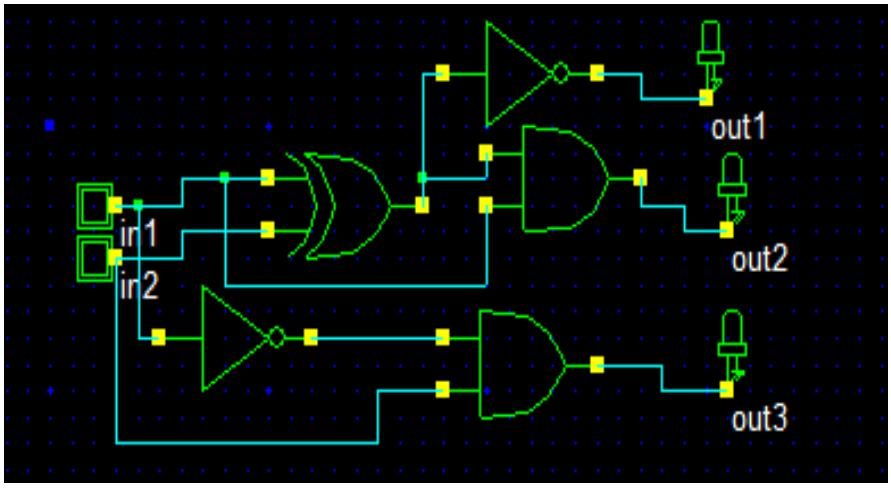

Figure 5. Implementation of Proposed-2 one-bit Magnitude comparator

The proposed model 2 shown in Figure 5 is a slight modification of proposed model-1 in Figure 4.This model is realized by replacing XOR gate by AND gate to get X greater than Y. The input X and difference output of half subtractor is given to AND gate to get X greater than Y. The logical expressions for every output is realized below. The difference of Half Subtractor is given to a NOT gate to get X equals to Y. Difference and input X is given to a AND gate to get X Greater than Y. And Borrow of Half Subtractor is equals to X Less than Y. This Proposed 2 model needs 2 AND gates, 2 NOT gates and 1 AND gate [12-15].

$$X<Y = \overline{X}Y$$

$$X = Y = \overline{\overline{X}Y + X\overline{Y}}$$

$$= \overline{\overline{X}Y}.\overline{X\overline{Y}}$$

$$= (X+\overline{Y})(\overline{X}+Y)$$

$$= XY + \overline{X}\overline{Y}$$

$$X>Y = (\overline{X}Y + X\overline{Y})A$$

$$= X\overline{Y}$$

2.3. Proposed Model-3

The proposed model 1, 2 and existing comparator have same number of logic gates. Proposed model-3 requires 4 logic gates shown in Figure 6.The output X greater than Y and the output X equals to Y both realization is similar to proposed model 2. In this model the input X and Difference output of Half Subtractor is given to AND gate to get X Less than Y. By modifying a circuit like this the number of gates required to design is reduced to 4 (as conventional comparator requires 5 gates).The logical expressions for every output is given below [16- 19].

The inputs X and Y are given to a XOR gate. The XOR output is given to a NOT gate to get X equals to Y. Input X and output of XOR is given to an AND gate to get X Greater than Y. Input B and output of XOR is given to an AND gate to get X Less than Y. This Proposed 3 model requires 2 AND gates, 1 NOT gate and 1 XOR gate [20- 22].

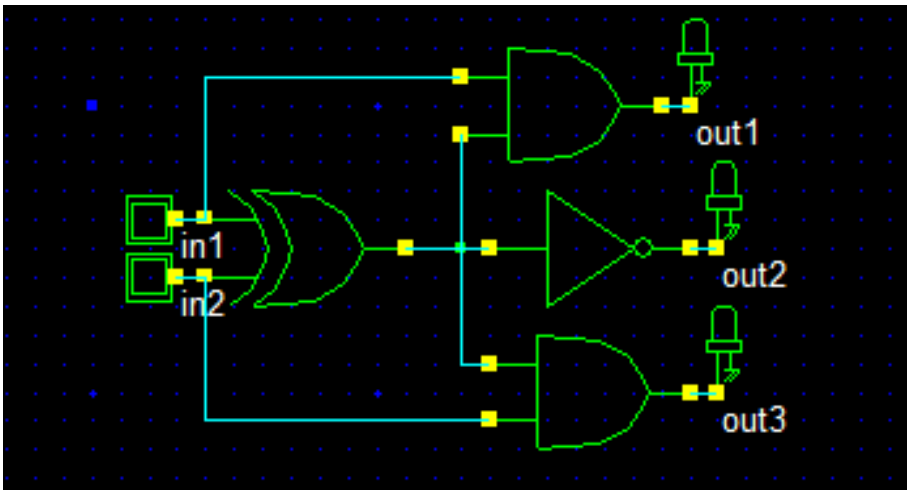

Figure 6. Implementation of Proposed-3 one-bit Magnitude comparator

$$X<Y = (\overline{X}Y + X\overline{Y})B$$

$$= \overline{X}Y$$

$$X = Y = \overline{\overline{X}Y + X\overline{Y}}$$

$$= \overline{\overline{X}Y}.\overline{X\overline{Y}}$$

$$= (X+\overline{Y})(\overline{X}+Y)$$

$$= XY + \overline{X}\overline{Y}$$

$$X>Y = (\overline{X}Y + X\overline{Y})X$$

$$= X\overline{Y}$$

2.4. Proposed Model-4

This model requires only 3 gates shown in Figure 7 and very simple to design and also the performance of this comparator is better interms of area, delay and power consumption compared to existing comparator. The input X and Y is given to XNOR gate to get X equals to Y output. The remaining two outputs are realized by using two NOR gates. To get X greater than Y output high the input Y and output of XNOR gate is given to NOR gate. The input X and output of XNOR gate is given as inputs to NOR gate to get X Less than Y. The logical expression for every output is given below [23-25]. The inputs X and Y is given to a XNOR to get X equals to Y. Input X and output of XNOR is given to a NOR gate to get X Greater than Y. Input A and output of XNOR is given to a NOR gate to get X Less than Y. This Proposed model-4 needs only XNOR gate and two NOR Gates [23-24].

$$\mathbf{X<Y} = \overline{XY + \overline{X\overline{Y}} + X}$$

$$= \overline{XY + \overline{X\overline{Y}}.\overline{X}}$$

$$=\overline{\overline{X\overline{Y}}}.\overline{XY}.\overline{X}$$

$$=(X+Y)(\overline{X}+\overline{Y})\overline{X}$$

$$=(\overline{X}Y)(\overline{X}+\overline{Y})$$

$$=\overline{X}Y$$

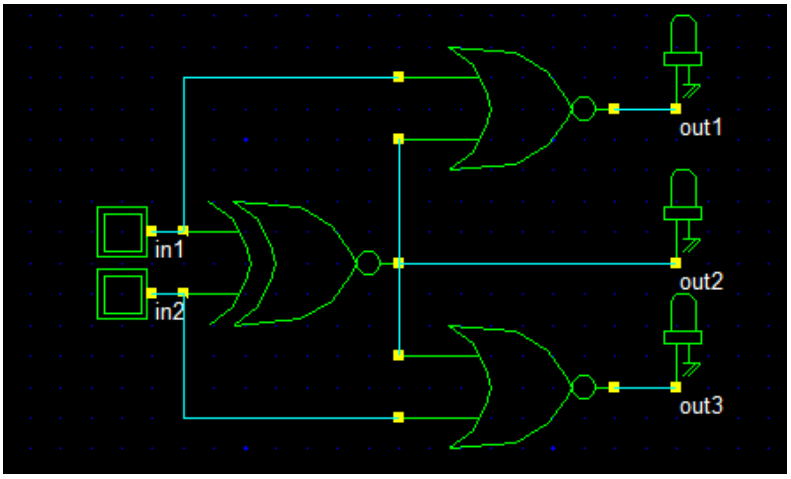

Figure 7. Implementation of Proposed Model-4 one-bit Magnitude comparator

$$X=Y = XY + \overline{X\overline{Y}}$$

$$X>Y = \overline{XY + \overline{X\overline{Y}} + Y}$$

$$= \overline{XY + \overline{\overline{X}\overline{Y}}.\overline{Y}}$$

$$= \overline{\overline{X}\overline{Y}}.\overline{\overline{X}\overline{Y}}.\overline{Y}$$

$$=(X+Y)(\overline{X}+\overline{Y})\overline{Y}$$

$$=(X\overline{Y})(\overline{X}+\overline{Y})=X\overline{Y}$$

3. RESULTS AND DISCUSSION

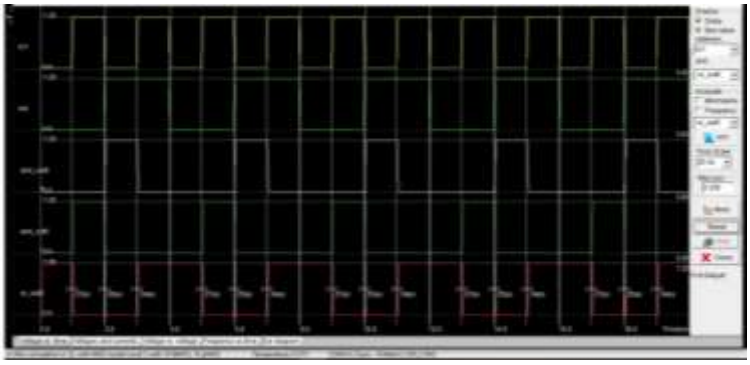

Figure 8. Timing Diagram of One Bit Comparator Existing Model in 120 nm Technology

The timing diagram shown in Figure 8 reveals that the average delay of existing one bit magnitude comparator is 25.7ps, power consumption 8.54µW and also it requires 20 transistors to implement in CMOS 120nm technology.

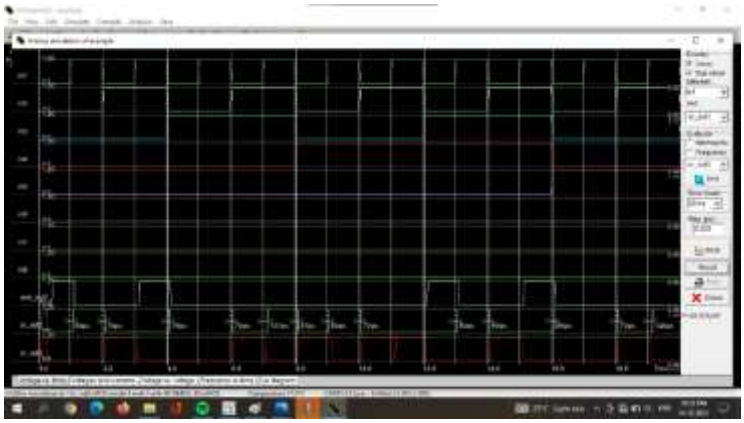

Figure 9. Timing Diagram of Four-Bit Comparator existing model in 120nm Technology.

The timing diagram shown in Figure 9 reveals that the average delay of existing four bit magnitude comparator is 117.83ps, power consumption is 45.03µW and it requires 178 transistors to implement in CMOS 120nm technology.

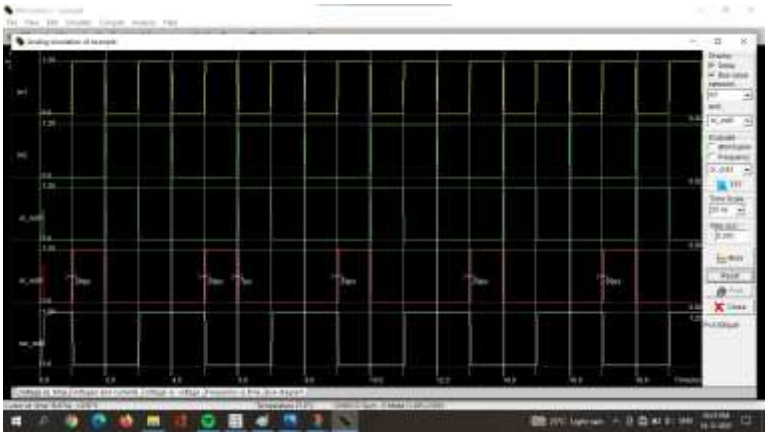

Figure 10. Timing Diagram of One Bit Comparator Proposed 4 Model in 120nm Technology

The timing diagram shown in Figure 10 reveals that the average delay of proposed model-4 one bit magnitude comparator is 15.5ps, power consumption is 3.55µW and it requires 14 transistors to implement in CMOS 120nm technology. The above results have better performance in terms of transistor count, power, delay than existing one bit magnitude comparator.

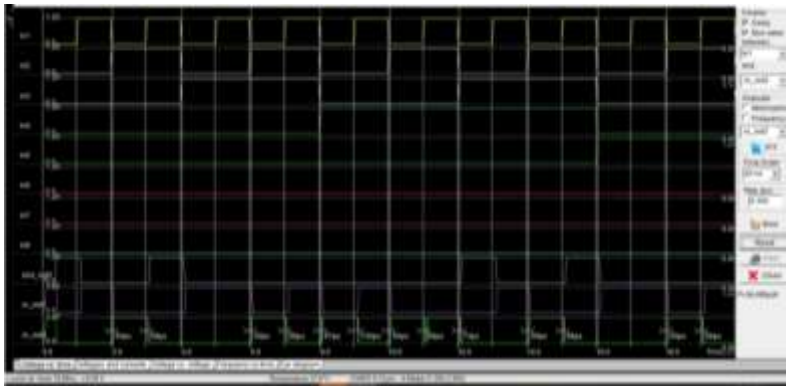

Figure 11 Timing Diagram of Four Bit Comparator proposed 4 Model in 120 nm Technology

The timing diagram shown in Figure 11 reveals that the average delay of proposed model-4 one bit magnitude comparator is 84.1ps, power consumption is 39.08µW and it requires 153 transistors to implement in CMOS 120nm technology. The above results have better performance interms of transistor count, power, delay than existing four-bit magnitude comparator.

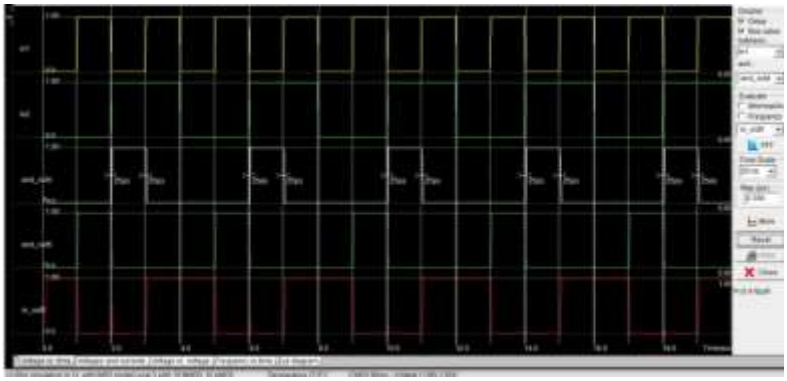

Figure 12. Timing Diagram of One Bit Comparator Existing Model in 90 nm Technology

The timing diagram shown in Figure 12 reveals that the average delay of existing one bit magnitude comparator is 23.16ps, power consumption 5.41µW and it requires 20 transistors to implement in CMOS 90nm technology.

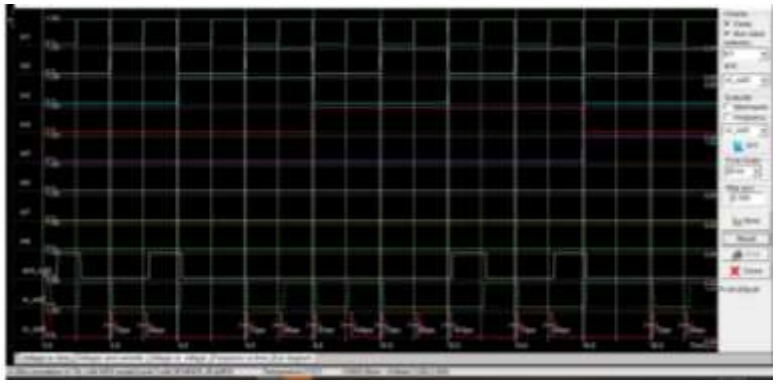

Figure 13. Timing Diagram of Four Bit Comparator Existing Model in 90 nm Technology

The timing diagram shown in Fig.13 reveals that the average delay of existing four bit magnitude comparator is 89.83ps, power consumption 30.95µW and it requires 178 transistors to implement in CMOS 90nm technology.

The timing diagram shown in Figure 14 reveals that the average delay of proposed model-4 one bit magnitude comparator is 14ps, power consumption is 2.37µW and it requires 14 transistors to implement in CMOS 90nm technology. The above results have better performance interms of transistor count, power, and delay than existing one bit magnitude comparator.

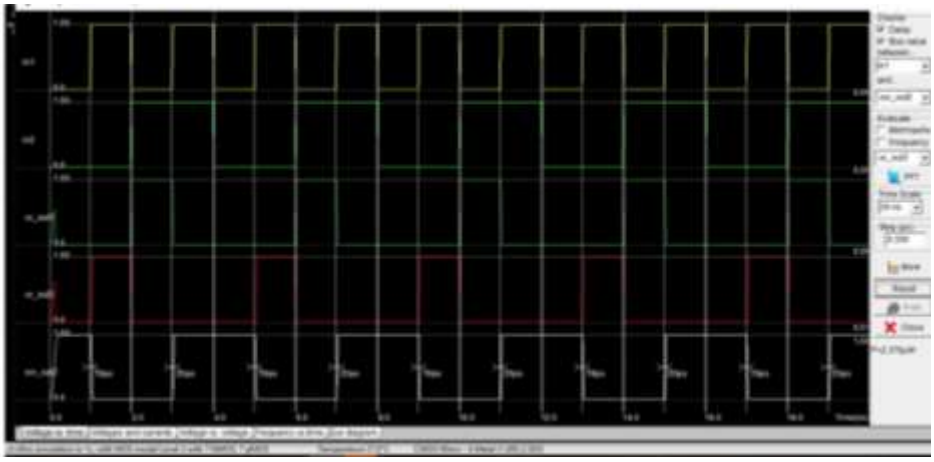

Figure 14. Timing Diagram of One Bit Comparator Proposed 4 Model in 90 nm Technology

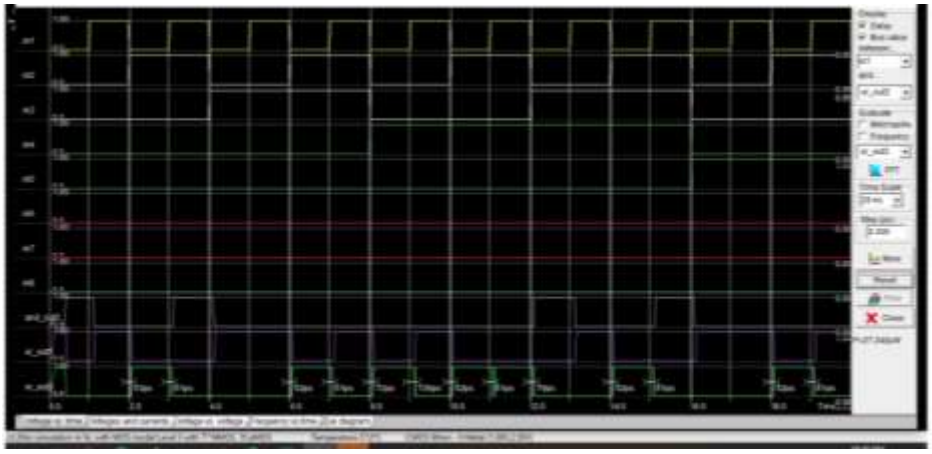

Figure 15. Timing Diagram of Four Bit Comparator Proposed 4 Model in 90 nm Technology

The timing diagram shown in Fig.15 reveals that the average delay of proposed model-4 four- bit magnitude comparator is 80.33ps, power consumption is 27.24µW and it requires 153 transistors to implement in CMOS 90nm technology. The above results have better performance interms of transistor count, power, delay than existing four- bit magnitude comparator.

The results shown in Table-3 and Table-4 shows that implementing proposed model-4 shown in Figure 7 in CMOS design have better performances in terms of transistor count, delay, power than the existing comparator in both 90nm and 120nm technologies. And also, it shows that implementing in 90nm technology have better results compared to 120nm technology.

Table 3. Comparison of one bit Magnitude Comparator with proposed model- 4 in 90nm and 120nm Technology

Technology used	90nm		120nm	
Parameters	**Existing Model**	**Proposed model- 4**	**Existing Model**	**Proposed model- 4**
No. of transistors	20	14	20	14
No. of logic gates	5	3	5	3
Power consumption (µW)	5.410	2.37	8.540	3.555
Delay (ps)	23.16	14	25.7	15.5

Table 4. Comparison of Four- bit Magnitude Comparator with proposed model- 4 in 90nm and 120nm Technology

Technology used	90nm		120nm	
Parameters	**Existing Model**	**Proposed model- 4**	**Existing Model**	**Proposed model- 4**
No. of transistors	178	153	178	153
No. of logic gates	41	33	41	33
Power consumption (µW)	30.952	27.240	45.031	39.080
Delay (ps)	89.83	80.33	117.83	84.1

4. CONCLUSION

The final results in terms of number of logic gates, transistor count, power consumption and delay have been obtained at 90nm and 120nm technologies. From the results designing a magnitude comparator using proposed model-4 design style reduce all parameters of transistor count, logic gates count, power consumption and delay of the comparator by 30% ,40%, 58.38%,38.688 % respectively for 1 bit comparator and 19.5%,14.05%,13.21%,28.088% respectively for four-bit comparator. And also implementing in 90nm technology have better performance than implementing in 120nm technology. All this simulation results have done in DSCH and microwind tools. Based on the following advantages in area, power and delay of the proposed model-4 magnitude comparator can be used for various applications such as scientific computations, VLSI designs, Test circuits etc. As per the results, the proposed model- 4 magnitude comparator is quite suitable for present day works.

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