Performance Analysis of $Si_{1-x}Ge_x$ Channel Based Double Gate Junctionless Transistor

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Abstract

A Silicon-Germanium channel based double gate junctionless transistor is demonstrated with 20 nm gate length. Mole fraction of germanium in SiGe channel is varied to understand the effect of germanium percentage in the device characteristics and opportunity of device performance optimization. Different characteristic like transfer characteristics, drain characteristics, transconductance, gate leakage current is evaluated for the junctionless transistor structures. Junctionless transistor with increasing germanium mole fraction demonstrated improvement in the device performance in all respect except the gate leakage current. To achieve appropriate threshold voltage the mole fraction of germanium in the SiGe can be adjusted. Performance of the $Si_{1-x}Ge_x$ channel junctionless device with gate dielectrics GeO_2 are compared for different mole fraction.

Keywords. Junctionless, mole fraction, transconductance, gate leakage current, TCAD, $Si_{1-x}Ge_x$.

1. INTRODUCTION

For decades researchers are involved in continuous improvement of semiconductor technology. In the race of down scaling of physical dimensions many critical issues are faced. These challenges need to be addressed to keep up the increment in switching speed and reduce power consumption [1-2]. Requirement of the ultra- shallow junction brings a challenge to the fabrication process [3]. In such context Junctionless transistor (JLT) was conceptualized and demonstrated by J. P. colinge et al. as a uniformly doped drain, channel and source region [4-6]. Ease of fabrication, absence of junction, and immunity to short channel effects made JLT attractive to the researchers. The Junctionless transistor conducts in accumulation mode and acts like a gated register. Study of SCEs [7-8], temperature effect [9-10], analytical modelling [11-12] of parameters for junctionless transistor was performed. Junctionless transistors have been tested for sensors and circuit applications [13-16]. Due to

developments in recent years, JLT been projected as an alternative of conventional MOSFET for future technology.

Still, some of the research has shown the inferior on-state current of junctionless transistor compare to the conventional MOSFETs [17]. Many techniques like use of high-k dielectric, multi-gate structure and gate stack are also employed to improve the on state current level of JLT. Use of group III-V compound or Ge in channel material can be an alternative to overcome the fundamental limitation of silicon technology [18-19]. But due to the lower quality of Ge epitaxy and fabrication difficulties, use of Ge channel has not become popular. Further inferior interface and unstable dielectric on the Ge epitaxy is also inherited. Due use of SiGe will be more suitable to get the advantages of high mobility and dielectric constant along with less interface trap problem of Ge. With merger of the advantages of Si and Ge, use of SiGe channel in junctionless transistor can play a big role in future technology. As SiGe properties changes with the percentage of the Ge, the requirement of study related to the mole fraction effect in junctionless characteristics is also inevitable. In this paper, performance of $Si_{1-x}Ge_x$ channel based junctionless transistor with double gate structure is studies for different mole fraction (x) of Ge.

2. Device Structure and Simulation Environment

The side view or cross-sectional view of the double gate junctionless transistor is shown in Figure 1. The terminals are named and marked in the figure. This symmetrical double gate structure is used for all the device simulations. As semiconductor wire thickness is kept low and double gate structure is used, the whole wire under gate will act like a channel. $Si_{1-x}Ge_x$ is used as a channel material and 1nm thick GeO_2 gate oxide is used in the device. The channel, source and drain regions are uniformly doped with 1.5×10^{19} atoms/cm^3. A thin gate oxide layer of 1 nm and semiconductor wire of 10 nm was considered to ensure the full depletion of the channel at the time of off condition. As the device works in accumulation mode, conduction will be done in bulk. In double gate structure entire semiconductor wire will act like a channel during its on-state. All the structural details are listed in the Table 1.

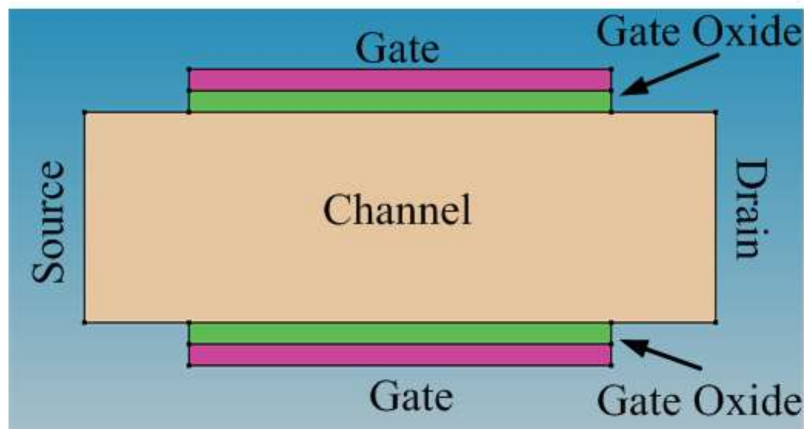

Figure 1. SiGe channel double gate junctionless transistor structure.

The thin body double gate junctionless transistors are simulated in the Synopsys Technology Computer Aided Design (TCAD). Structure editor is used to design the 3D structure. S device tool is used to simulate the structure for different condition with the help of carrier transport models, generation-recombination models, mobility models and tunnelling models. Further the results of the simulation are viewed with the help of S visual and inspect tool. Proper material parameters are also been included at the time of simulations. Work function of the gate material polysilicon (4.4eV) is specifically mentioned in the device physics section. Leakage current model also been included in the physics section of the simulator to estimate the gate leakage for the structure.

Table 1. Structural parameters of SiGe channel DGJLT

Sl. No	Parameter	Material Type	values
1	Channel length	$Si_{1-x}Ge_x$	20 nm
2	Channel Width	$Si_{1-x}Ge_x$	12 nm
3	Channel thickness	$Si_{1-x}Ge_x$	10 nm
4	Doping	Arsenic	1.5×10^{19} atoms/cm^3
5	Gate oxide Thickness	GeO_2	1 nm
6	Gate Contact	Polysilicon	4.4eV
7	Mole fraction (x)	$Si_{1-x}Ge_x$	1 to 0

3. RESULTS AND DISCUSSION

The proposed thin-body double gate structured SiGe channel junctionless transistor is simulated for gate voltage from -0.6V to 2 V. The mole fraction (x) of $Si_{1-x}Ge_x$ is changed from 0 to 1. With the change in quantity of Ge in SiGe the junctionless transistor characteristics also changes. It is observed that the DGJLT with germanium channel (x=1) shows better characteristics compare to DGJLT with Si channel (x=0). The transfer characteristics of DGJLTs are shown in Figure 2. With increment in mole fraction(x) of Ge the overall drain current increases and it also affect the threshold voltage. The threshold voltage moves towards the positive side with the increment in mole fraction of Ge. So increase in mole fraction of Ge makes the device more suitable for CMOS circuit applications.

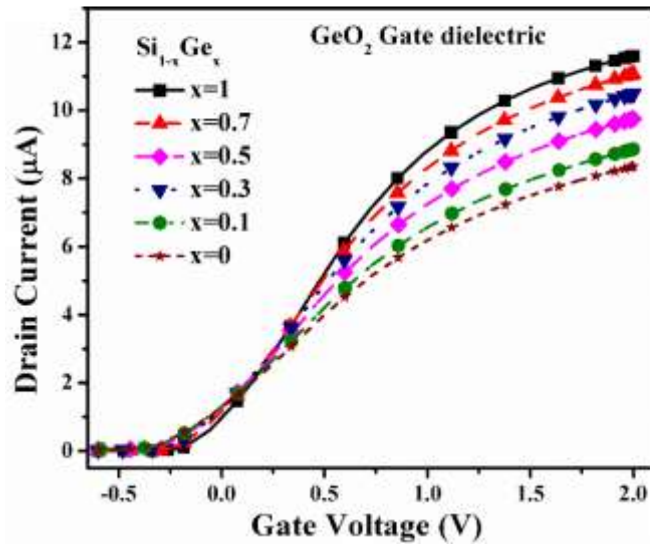

Figure 2. Transfer characteristics of $Si_{1-x}Ge_x$ channel DGJLT with GeO_2 gate oxide.

The transfer characteristics of DGJLTs in log scale are shown in Figure 3. It clearly shows the effect of mole fraction of Ge in the steepness of the curve in the subthreshold region. Degree of more steepness in the curve is better for analog and digital circuit applications. Device with higher steepness in the subthreshold region will require less gate voltage to sweep the device from off to on-state. Thus $Si_{1-x}Ge_x$ channel DGJLT with higher x value gives better subthreshold swing. Further increase in x value also shows improvement in Ion/Ioff ratio for the $Si_{1-x}Ge_x$ channel DGJLT.

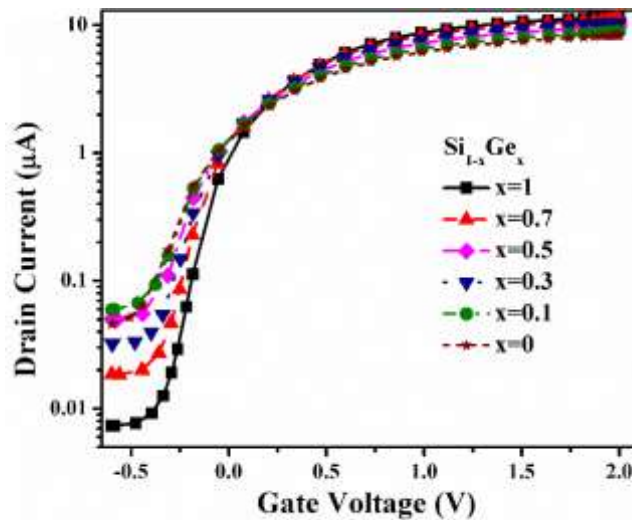

Figure 3. Steepness of transfer characteristics of $Si_{1-x}Ge_x$ channel DGJLT with GeO_2 gate oxide.

The drain characteristics of $Si_{1-x}Ge_x$ channel DGJLT with GeO_2 gate oxide is shown Figure 4. It shows that the mole fraction have effect in drain saturation current also. In saturation

region the drain current for higher x value changes less with change in drain voltage. As the results shows drain characteristics is more independent of drain voltage at the saturation, it is obvious that the $Si_{1-x}Ge_x$ channel DGJLT with higher x value will show better drain induced barrier lowering.

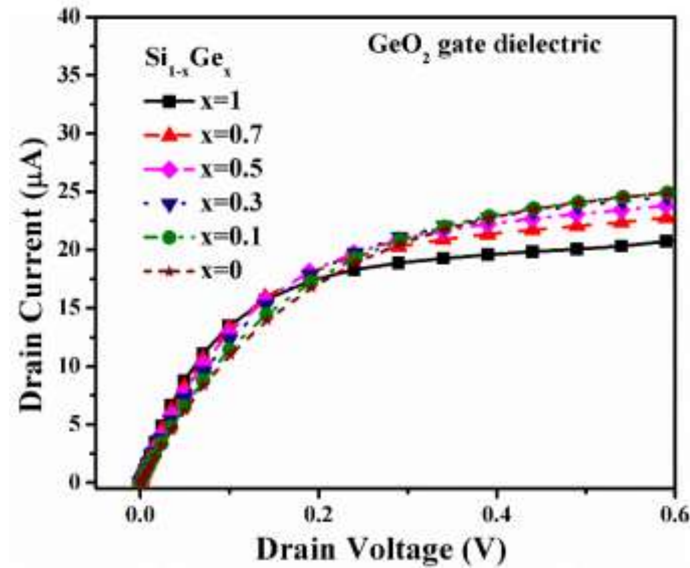

Figure 4. Drain characteristics of $Si_{1-x}Ge_x$ channel DGJLT with GeO_2 gate oxide.

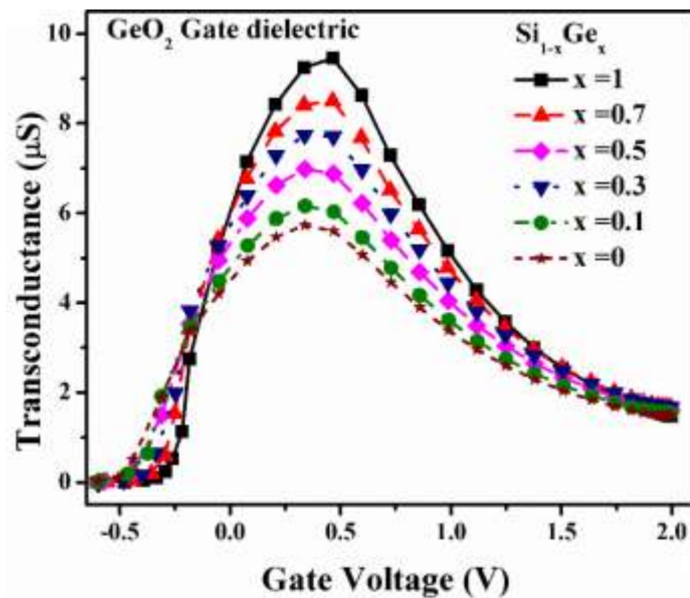

Figure 5. Transconductance of $Si_{1-x}Ge_x$ channel DGJLT with GeO_2 gate oxide.

As transconductance is a very important parameter for the device performance, it was evaluated for $Si_{1-x}Ge_x$ channel DGJLT with GeO_2 gate oxide. Figure 5 shows the transconductance of $Si_{1-x}Ge_x$ channel DGJLT as a function of gate voltage. High Ge

percentage in $Si_{1-x}Ge_x$ exhibits better transconductance. The details of the transconductance, threshold voltage, and on current are shown in Table 2. For mole fraction x=1, $Si_{1-x}Ge_x$ channel DGJLT showed maximum on current of 11.59 µA at V_{GS}= 2 V. Change in the threshold voltage of the devices with the change in germanium mole fraction shows that threshold voltage can be tailored with the help of mole fraction adjustment. Overall it helps the designer to optimize the junctionless transistor performance for future applications. Desired threshold voltage and current characteristics can be achieved with proper adjustment in mole fraction of the $Si_{1-x}Ge_x$ semiconductor material.

Table 2. Parameters of $Si_{1-x}Ge_x$ channel DGJLT with GeO_2 gate oxide.

Sl. No.	Mole fraction of $Si_{1-x}Ge_x$	Threshold Voltage, Vth (V)	Ion at V_{gs}=2V (µA)	g_m (µS)	V_{gm} (V)
1	x=1	-0.052	11.59	9.458	0.464
2	x=0.7	-0.099	11.07	8.503	0.463
3	x=0.5	-0.1293	10.49	7.743	0.336
4	x=0.3	-0.156	9.75	6.984	0.338
5	x=0.1	-0.183	8.85	6.162	0.339
6	x=0	-0.197	8.35	5.731	0.337

Figure 6 shows the gate leakage current of $Si_{1-x}Ge_x$ channel DGJLT for different mole fraction variation. With increased gate voltage gate leakage current also increases in all the junctionless devices. As germanium has lower energy bandgap compare to silicon, increasing mole fraction of Ge in $Si_{1-x}Ge_x$ channel leads to increase in gate leakage current. It is observed that the on-state gate leakage current increases in SiGe channel JLT compare to Si JLT. But the gate leakage current for all these devices are quite low with respect to the off state drain current, observed in Figure 3.

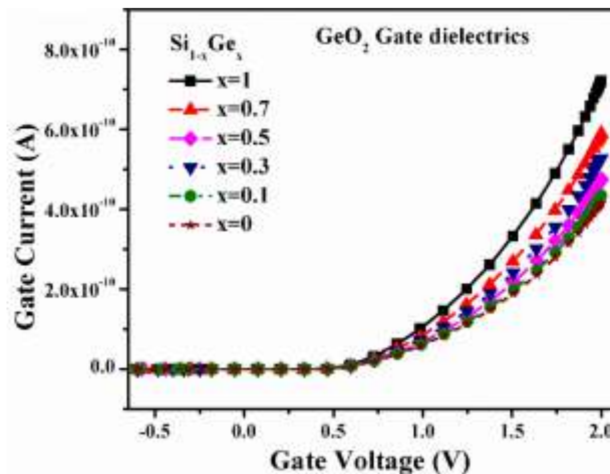

Figure 6. Gate leakage current of $Si_{1-x}Ge_x$ channel DGJLT with GeO_2 gate oxide.

4. Conclusion

This paper demonstrates a detailed device performance analysis of $Si_{1-x}Ge_x$ channel DGJLT with GeO_2 gate oxide. Simulation and analysis of different characteristics of the JLT with

different mole fraction of Ge were performed. $Si_{1-x}Ge_x$ channel JLT shows typical MOSFET characteristics. Change in mole fraction in $Si_{1-x}Ge_x$ has affect in all the device characteristics. Higher Ge percentage improves the threshold voltage, gives higher on-state current and transconductance. As increase in on-state gate leakage current stays under permissible limit, $Si_{1-x}Ge_x$ channel can be used in JLT with proper optimized performance to meet the future requirements of CMOS technology.

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