Designing of Low Power Ring Oscillator with Less Phase Noise for Frequency Synthesizers by using FINFET Techniques

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Abstract

This research presents a FinFET ring oscillator with adaptive leakage power minimization and reduction in Phase noise margin for Optical energy harvesting. Because these are battery-operated devices, an adaptive body biasing-based leakage power reduction optimizes the optoelectronic biomedical device's leakage power consumption. A five-stage ring oscillator with a frequency of 1 kHz was used to produce the requisite oscillation frequency. The suggested ring oscillator was constructed and Spectre in Cadence Virtuoso Analog Design Environment (ADE) was used to mimic phase noise using 20nm FinFET technology. The suggested ring oscillator's supply voltage is fixed at 50 mV to reduce dynamic and leakage power consumption. The suggested ring oscillator consumes only 41.98 nW of dynamic power, which is 20% less In comparison to the conventional CMOS ring oscillator. The suggested ring oscillator has a leakage power consumption of 4.25 pW. The suggested low-leakage ring oscillator surpasses the competition and is better suited to low-power implantable biomedical devices. The suggested ring oscillator has a phase noise of -156.5 dBc/Hz at 1000 Hz offset frequency and a simulated temperature of 27°C compared to the existing CMOS ring oscillator which is - 114dBc@600KHz.

Keywords- Body Biasing, Optical Energy Harvesting, FINFET, Leakage Power, Ring Oscillator, Phase Noise, Jitter

Introduction

When we convert the optical energy from a laser source using the photo voltaic cell to electrical energy it will be ofthe order of microvolts [1]. To boost up this
energy we gofor an Energy harvesting system. One of the major components of Optical energy harvesting systems is oscillators. This paper is focused on the oscillators which play a major role in Energy harvesting. Oscillators are used in Charge pumps (CP),DC-DC Converters, Phase-Locked-Loop (PLL), etc.

An oscillator can take many forms, such as a ring oscillator or a harmonic oscillator. Harmonic oscillators are very complex and generate stable frequencies with high-quality factors (Q), but they consume a lot of power. Battery-operated implantable biomedical devices cannot be used with them. Ring oscillators, in contrast, are based on very simple circuits and consume very little power, so they are better suited to implantable biomedical systems.

Ring oscillators are used to synchronize the computation processes in any digital system. Ring Oscillators Have a Wide oscillation range, Smaller Size, and Highly integrated multiphase output compared to LC Voltage Controlled Oscillators. Harmonic oscillators provide a stable frequency with a very high-Quality factor but they consume very high power, which isnot suitable for battery-operated devices. Hence Ring oscillators are chosen which consume very less power and are very simple to design. The area occupied by the Ring Oscillator is very less thereby it improves the cost and yield hence well suited for Implantable bio Medical Devices.

In a Ring Oscillators Inverters in an odd number are connected in series with a positive feedback circuit forming a closed loop. This feedback from its last output to the input causes the oscillations There are two different voltage levels 1 or 0 and the output oscillation occurs between these two voltage levels. From this output oscillation, the speed is calculated. The number of inverters defines the stages in the ring oscillator. Say, for instance, if the number of inverters used is three, then it is referred to as a three-stage oscillator. Required output frequency defines stages of inverters in designing the oscillator. If an oscillator is developed with a single inverter, there are no sufficient output oscillations and gain. Random fluctuations in the phase of frequency-domain representation corresponding to time-domain variations from perfect periodicity are known as phase noise in signal processing("jitter"). In general, radio-frequency engineers refer to an oscillator's phase noise.

Varied degrees of periodicity or deviations in periodicity results in Phase noise. Phase noise increases at harmonic frequencies. As the additive noise is so close to the oscillation frequency, it cannot be filtered out. Nonlinear oscillators with well-designed limit cycles will be stable.

In Section II, This article discusses the analysis of phase noise in ring oscillators, and the design of the ring. At the end of the paper, we present the conclusion in section 3.

1. RELATED WORK

[1] Energy harvesting using the hybrid solar/laser light and working of outdoor SC based on storage for self sufficient operation is examined in this work. According to the manufacturer, SC requires the power of 10 W. Millimeter-wave phased-array transceivers are state-of-the-art.

[2] Organic photovoltaic (OPVs) are demonstrated can harvest power for optical wireless data receivers. Furthermore, because their band gap is greater than that of silicon, these OPVs are particularly interesting for indoor applications, as they can better match the spectrum of artificial light. An appropriate combination of a narrow band gap donor polymer and a no fullerene acceptor produces stable OPVs with a power conversion efficiency of 8.8 percent under 1 Sun and 14 percent under indoor illumination conditions.

[3] The photo voltaic effect, which is underutilized in modulators, Optical modulators use semiconductors with light as input and generate electrical energy. This effect is used to show a silicon modulator that uses sub- a/bit electrical energy at sub - GHz rates, which is useful for massively parallel input/output systems such as brain interfaces.

[4] Briefs about the energy harvesting system with a fault-tolerant method and also give the role of oscillators in the energy harvesting system.

[5] For particular power consumption limitations, this paper presents a paradigm for assessing CMOS ring oscillatorphase noise. Both linear and nonlinear operations are taken into account in this model. It implies that for minimal phase noise, quick rail-to-rail switching is required, as well as up-conversion. The current bias/ control circuit's low-frequency noise can have a big impact. This phase noisemodel has been verified using Results of simulation and measurement, In addition, it had a phase noise of 114dBc/Hz coupled-ring oscillator.

2. PURPORTED TIME-DELAY OSCILLATOR

The purported low leakage 5-stage time-delay oscillator has been designed using 20nm FinFET technology. The schematic of the purported time-delay oscillator has been explained. Design of W/L ratio for FinFET inverter. The most important parameter in the Time-delay oscillator is the Threshold voltage (VTH) of the nMOSFET in the inverter. Required VTH can be obtained by properly designing the value of W and L of nMOSFET based on the inverter ratio which is given by equation (7)

$$K\pi = \kappa\pi\,(2)/\kappa\theta * \kappa\sigma \quad \text{----(1)}$$

Where $K\pi$ is the Inverter ratio
$K\theta$ An aspect ratio of nMOSFET
$K\sigma$ is the Aspect ratio of pMOSFET

This 5-stage oscillator uses five inverters to produce therequired oscillation of 1KHz frequency. Adaptive Body Bias can compensate and achieve more uniform transistor performance despite the variations. In the purported low leakage FinFET time-delay oscillator, The maximum leakage Where Kr is the Inverter ratio Kn is the aspect ratio of nMOSFET Kp is the aspect ratio of pMOSFET. Current in the cutoff is given by the nMOSFET hence it is the main leakage power contributor limit leakage power, the inverter's nMOSFET bulk terminal is coupled to a negative bias voltage source via a pMOSFET.

When the nMOSFET is in the cut-off state, a negative bias voltage is provided to raise the threshold voltage. Because the thresholdvoltage and leakage power consumption are inversely proportional, the leakage power consumption

during the NMOSFET cutoff state can be considerably reduced.

Where μn is the electron mobility
Cox is the oxide layer capacitance
W is the FinFET device-width
L is the FinFET device Length

Similarly Eqn 2 $K_p * Tp\, C_{ox}$ ----------(2)

Where μn is the electron mobility and Cox is the oxide layer capacitance.

Substituting Equation (2) and (3) in equation (1) we get the frequency of operation of the time-delay oscillator can be calculated.

The value of L is 20nm from the FinFET library. Hence Wp will be equal to twice that of Wn. The Value of W for nMOSFET is chosen as 50nm hence the value of W for pMOSFET is 100nm. By considering the designed parameter values given in Table 1 the required Threshold voltage and the propagation delay are obtained.

TABLE I DESIGN PARAMETERS OF FinFET INVERTER USED IN PURPORTED TIME-DELAY OSCILLATOR

Wp(nm)	100
We(nm)	50
L(nm)	20

The W/L ratio affects the Time-delay oscillator's Phase Noise Margin. The Phase noise Margin in the Purported Time-delay oscillator is improved by using adaptive body biassing and designed W/L values. The output of the purported low leakage 20nm FinFET time-delay oscillator has been displayed in Figure. 3. The time-delay oscillator produces the square wave with a 50% duty cycle at its output terminal. The input terminal is given with the same output. Hence the time-delay oscillator produces a square wave continuously. The operating frequency is determined by the propagation delay (Td) and the number of stages (N) of the time-delay oscillator.

When the supplied supply voltage is 500mV and the simulated temperature is 27 C, the purported time- delay oscillator has a frequency of 1KHz. To reduce dynamic and leaky power consumption, the minimal supply voltage was chosen to operate the suggested ring oscillator in a low swing.

SIMULATION RESULTS AND DISCUSSION

The design and simulation of the purported work are using 20nm FinFET technology with Cadence Virtuoso Analog Design Environment (ADE) EDA tools. The high-speed spice simulator ‘Spectre’ is used to plot the output waveforms. The simulation parameters which are used to characterize the purported ring oscillator have been listed in Table II. The time-delay oscillator circuit has been simulated with 500mV supply voltage when the simulation temperature is 27oC. Transient simulation has been performed to plot the output waveform.

TABLE III INFLUENCE OF FREQUENCY ON PHASE NOISE

Frequency (Hz)	Phase Noise in dBc/Hz
1	-135
5	-138
10	-144
50	-149
100	-152
500	-153
1000	-156.5

TABLE IV INFLUENCE OF TEMPERATURE ON OSCILLATOR FREQUENCY

Temperature (°C)	Frequency (kHz)
-25	0.948
0	0.964
25	0.983
27	1
50	1.025
75	1.046
100	1.067
125	1.094

Random fluctuations in a waveform's phase, corresponding to time-domain deviations from perfect periodicity, are represented in the frequency domain as phase noise ("jitter"). The Phase Noise of the Time- delay oscillator is -156.5 dBc/Hz at 1000 Hz offset frequency, and the simulation temperature is 27°C. Phase noise is a type of specification in the frequency domain that implies short-term frequency stability. -dBc/Hz is the phase noise unit. Thus, at offset frequency, the offset is -156.5dBc/Hz @ 1000 Hz. When the frequency offset is 1000 Hz, the phase noise is -156.5dBc/Hz. A higher absolute value of phase noise is preferable. Frequency is varied from 1Hz to 1000Hz and the value of Phase noise have been listed in Table III.

The influence of temperature on the frequency of the purported time-delay oscillator has been analyzed by varying the simulation temperature from -25 oC to 125 oC with the step value of 25 oC. The measured values have been listed in Table IV. When the temperature is -25 oC, the oscillator frequency is 0.948 kHz. At room temperature (27oC), the value of oscillator frequency is1 kHz. When the temperature reaches 125 oC, the oscillator frequency is 1.094 kHz. The temperature sweep analysis shows that the oscillator frequency is directly proportional to the temperature.

The Influence of frequency on the Phase noise of the purported time-delay oscillator has been plotted by varying the frequency from 1Hz to 1000Hz. As the simulation frequency increases, the phase noise of the time-delay oscillator decreases.

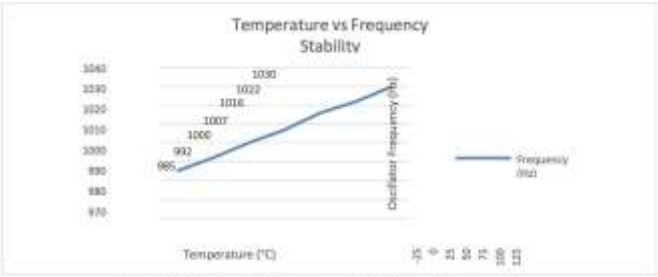

Figure 5. Influence of Temperature on Oscillator Frequency

TABLE V SIMULATION PARAMETERS

Item	Description
EDA Tool	Cadence Virtuoso ADE
Simulator	Specter
Technology	20nm FinFET
Supply Voltage	500mV
Simulation Temperature	27 °C

The influence of temperature on the Oscillation frequency of the purported time-delay oscillator has been plotted by varying the simulation temperature from -25 C to 125 C. As the simulation temperature increases, the oscillation Frequency of the time-delay oscillator increases exponentially as shown in Figure. 5. It gives an astable Frequency of 1KHz at a temperature of 27 C.

The performance metrics of both existing and purported 5-stage time-delay oscillators with 1 kHz operating frequency are analyzed and compared. They are listed in Table V. The purported time-delay oscillator has been designed in 20nm FinFET technology whereas the existing time-delay oscillator circuit was implemented in 0.5µm CMOS technology. The power supply of the purported time-delay oscillator and the existing time-delay oscillator are 500mV and 2.5V respectively. The power consumption ofthe purported time-delay oscillator and the existing time-delay oscillatorare 41.98nW and 150µW respectively.

TABLE VI PERFORMANCE COMPARISON

Parameters	Purported	Existing [1]
Technology	20nm FinFET	0.5µm CMOS
EDA Tool	Virtuoso ADE	Tanner
No. of Stages	5	3
Power Supply (V)	500 mV	2.5 V
Power Consumption (W)	41.98 NW	150 µW
Oscillator Frequency (Hz)	1000	600K
Simulation Temperature	27 ℃	27 ℃
Phase Noise	-156.5dBc@1000Hz	-114dBc@600KHz
Analysis	Transient	Transient

CONCLUSION

This study proposes and implements an adaptive leakage power minimization based FinFET time-delay oscillator with a stable frequency of 1kHz and improved noise performance which is more suitable for Optical Energy harvesting. Since this oscillator produces a stable oscillation, optical energy is harvested without noise. A leakage power minimization method based on adaptive body biasing has been suggested. A time-delay oscillator of five-stage with a frequency of 1 kHz was used to obtain the oscillation frequency. 20nm FinFET technology is used to design the recommended oscillator. 500mV of input reduces dynamic and leakage power consumption. The purported time-delay oscillator consumes only 41.98 nW of dynamic power in comparison to the existing CMOS time-delay oscillator consumes 50 W of power, whereas. The purported time-delay oscillator has a very low leakage power of 4.25 pW. The phase noise of the planned time-delay oscillator is - 156.5dBc/Hz.

REFERENCES

[1] John Fakidis_, Stefan Videv_, Stepan Kuceray, Holger Claussenz, and Harald Haas, “On the design of Optical Energy Harvesting and storage system for outdoor small cells” IEEE Interantional Conference on communication,Apr 2022Iman Tavakkolnia et all,
“Organic photovoltaics for simultaneous energy harvesting and high-speed MIMO optical wirelesscommunications” Official journal of the CIOMP 2047- 7538
[2] M. de Cea 1, A. H. Atabaki1 & R. J. Ram “Energy harvesting optical modulators with subattojoule per bit electrical energy consumption”
Nature Communcation, Apr 2021
[3] Jeneetha Jebanazer, J, Janaki Rani, M.Anand 2021, ‘ Enhanced Energy Harvesting System for Implantable Bio-Medical Devices with Fault Tolerance’, Journal of Green Engineering, vol. 11, no.1, pp 746-767
[4] Liang Dai and Ramesh Harjaani, “Analysis and Design of Low Phase noise Ring Oscillator,” IEEE conf, ISLPED'00, pp. 289-294,
Jul 2002.
[5] A. B. Islam, “Design of wireless power transfer and data telemetrysystem for biomedical applications,” Ph.D. dissertation, Dept. Elect. Eng. Comput. Sci., Univ. Tennessee, Knoxville, TN, USA, 2011.
[6] C. Lu, V. Raghunathan, and K. Roy, “Efficient design of micro-scale energy harvesting systems,” IEEE J. Emerg.

Sel. Topics Circuits Syst., vol. 1, no. 3, pp. 254–266, Sep. 2011.

[7] Sahakoon Panyai, Apinunt Thanachayanont, “ Design and Realization of a Process and Temperature Compensated CMOS Ring Oscillator ”, 2012. *Internal Startup Circuit for Pacemakers", IEEE Transactions On Very Large Scale Integration (VLSI)*

Biography

M. Lenin Kumar received the bachelor's degree in Electronics and Communication Engineering from Anna University in 2011, the master's degree in Electronics and Communication Engineering from Anna University in 2013, and the philosophy of doctorate degree in Electronics & Communication Engineering from Dr MGR University in 2021, respectively. He is currently working as an Assistant Professor at the Department of Electronics and Communication, Faculty of Engineering, Chandigarh University. His research areas in underwater wireless communication and modems. He has been serving as a reviewer for many highly-respected journals.