LC Oscillator Structures

2.1 Introduction

The oscillators are the only block that is universally used in both transmit and receive paths (see Figure 2.1), and consequently their spectral purity and efficiency highly affect the transceiver performance. The phase noise of the oscillator results in reciprocal mixing in the receive path, where the blocker is mixed with the oscillator's phase noise and shows itself on top of the desired signal and consequently degrades the receiver sensitivity [1]. This problem especially shows itself in contemporary mobile phones that support 2G, 3G, and 4G modes and WiFi standards with two very close antennas in one device [2], or in wide-band CMOS receivers without off-chip SAW filters, in which blockers can enter the chip without any pre-attenuation [3]. In transmit path, the amplified phase noise of the transmitter's oscillator can desensitize a nearby receiver [1]. Furthermore, as one of the most power hungry blocks in the transceiver, its power consumption limits the efficiency of the transceiver [4, 5]. Therefore, understanding and modeling the phase noise of an oscillator have been the subject of numerous studies [6–12]. The linear time-variant model through the impulse response of each noise source of the oscillator [10] is the most approached method since its introduction.

We are relying on this method to analyze the oscillators in this book; so let us have a quick overview first. The relatively accurate modeling of phase noise in this method is by acknowledging time-variant behavior of the oscillators. To make it more clear, note that a current impulse injected to the tank of Figure 2.2(a) can change oscillation phase and/or amplitude depending on the injection time (see Figure 2.2(b,c)). If the current impulse is injected when oscillation waveform is at its maximum, the oscillation amplitude will be disturbed but the phase will not be. On the other hand, current impulse at the zero-crossings results in a minimum amplitude and maximum phase disturbance. The impulse response is however periodic with respect

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Figure 2.1 A generic RF transceiver [1].



Figure 2.2 Phase response to an impulse current [10].

to injection time. The impulse sensitivity function (ISF), $\Gamma(\omega_0 \tau)$, is defined as a dimensionless, periodic function with period of 2π that describes the oscillation phase shift from injected current impulses during the period [10]. ISF is a periodic function and, consequently, can be written in a Fourier series,

$$\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{i=1}^{\infty} c_n \cos(n\omega_0 t + \theta_n).$$
(2.1)

Phase modulation is then obtained by convolving the current noise source and ISF as

$$\phi_n(t) = \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^t i(\tau) + \sum_{i=1}^\infty c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0 t + \theta_n) \right], \quad (2.2)$$

where q_{max} is the maximum charge displacement at the capacitance of the node that the noise is injected.

For a current such as $i(t) = I_n \cos[(n\omega_0 + \Delta\omega)t]$, the excess phase can be found as

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta \omega)}{2q_{max} \Delta \omega}.$$
(2.3)

The modulated phase shows itself in the phase noise spectrum since we can write

$$x(t) = A\cos(\omega_0 t + \phi_n(t)) \approx A\cos(\omega_0(t)) - A\phi_n(t)\sin(\omega_0 t), \quad (2.4)$$

and consequently this injected current results in two sidebands at $\omega_0\pm\Delta\omega_0$ and

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{I_n c_n}{4q_{max}\Delta\omega}\right)^2.$$
 (2.5)

The same method can be generalized for random noise sources and by applying the Parseval's relation to derive the phase noise for a white power spectral density noise as,

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{\frac{i\bar{n}}{\Delta f}\frac{1}{2\pi}\int_{0}^{2\pi}\Gamma^{2}(\phi)d\phi}{4q_{max}^{2}\Delta\omega^{2}}\right).$$
(2.6)

The most accurate method to calculate ISF of each noise source is by simulation. An impulse current should be injected to a node in the circuit at a certain time. The time shift of the oscillation should be measured after a few cycles and be converted to the phase shift. By sweeping the injection time of the current impulse over one oscillation period, ISF can be measured. Very recently, a fast and accurate simulation technique of ISF based on positive sidebands of periodic transfer function (e.g. PXF in Cadence) was revealed in [13].

Upconversion of the device's 1/f noise to phase noise can also be investigated by this method.

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If the application demands a low phase noise, the LC oscillator structure should be chosen. The thermal to phase noise upconversion (20 dB/dec region) of these oscillators can be found as

$$\mathcal{L}(\Delta\omega) = 10 \log_{10} \left(\frac{R_t kT}{2Q_t^2 V_{OSC}^2} \cdot F \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \right)$$

= $10 \log_{10} \left(\frac{kT}{2Q_t^2 \alpha_I \alpha_V P_{DC}} \cdot F \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2 \right),$ (2.7)

where R_t is the equivalent parallel resistance of the tank, k is Boltzmann's constant, T is the temperature, $\alpha_V = \frac{V_{osc}}{V_{DD}}$ and $\alpha_I = \frac{I_{\omega_0}}{I_{DC}}$, and F is the noise factor and can be found as

$$F = \sum_{i} \frac{R_t}{2kT} \cdot \frac{1}{2\pi} \int_0^{2\pi} \Gamma_i^2(\phi) \,\overline{i_{n,i}^2(\phi)} \,d\phi, \qquad (2.8)$$

in which Γ_i is the ISF of the *i*th noise source.

2.2 Class-B Oscillator Topology

The traditional class-B oscillator, of Figure 2.3(a), is widely used in RF applications due to its simplicity and robustness. The noise factor in a class-B structure is ideally equal to $\gamma + 1$ [12] if M_T tail current transistor is an ideal current source. In this case, not only the current source avoids contributing to phase noise, but it also provides an infinite impedance at the common source of the g_m transistors, which, as we explain later, is beneficial for the phase noise reduction. Let us investigate how the performance of this oscillator topology can be improved. The figure of merit (FoM) that is widely used to compare the oscillator performance is

$$FoM = |PN| + 20\log_{10}(\omega_0/\Delta\omega) - 10\log_{10}(P_{DC}/1mW).$$
(2.9)

The objective is to reduce the phase noise and/or power consumption of the oscillator.

Increasing the tank's quality factor reduces the oscillator's phase noise. The tank's quality factor depends on both the inductive and capacitive quality factors:

$$\frac{1}{Q_t} = \frac{1}{Q_L} + \frac{1}{Q_C}.$$
(2.10)

The inductor's quality factor, Q_L , which usually limits Q_t , is mostly technology-dependent but does not improve with technology scaling. The



Figure 2.3 A class-B oscillator (a) schematic; (b) oscillation amplitude versus tail current; (c) ideal and real drain current waveforms; (d) oscillation voltage waveforms.

capacitive quality factor, Q_C , on the other hand, depends on the tuning range of the oscillator. The switched-capacitor structure shown in Figure 2.4 is often used to tune the conventional oscillators. When M_s is on, $C_{on} = \frac{C}{2}$, and the switch's on-resistance, r_{on} defines $Q_C = \frac{1}{2r_{on}C\omega}$. To improve Q_c , r_{on} and consequently M_s size should increase. However, a larger M_s would add to the parasitic capacitance and consequently would increase the switched-capacitor equivalent capacitance when M_s is off: $C_{off} = \frac{CC_{par}}{2(C+C_{par})}$. Consequently, Q_t will be defined by the technology and oscillator's tuning range, and is rarely a design parameter to substantially improve the phase noise.

Another approach to improve the oscillator's phase noise is by reducing the tank's inductance while keeping its quality factor the same. Doing so



Figure 2.4 The switch capacitor tuning circuit in on and off states.

reduces $R_t = L\omega Q_t$; however, it increases the power consumption $P_{DC} =$ $\frac{V_{OSC}^2}{\alpha_V \alpha_I R_t}$, with the same rate, and hence FoM will not improve. Furthermore, by reducing the inductor's size, the tank interconnection losses become more important and, at some point, they will limit its quality factor. This oscillator shows the best performance when its oscillation amplitude is around V_{DD} [14–16] and consequently $\alpha_V = 1$. After this point, the oscillation amplitude stops increasing with the tail current increase (see Figure 2.3(b)) while its power consumption still increases linearly with the tail current, thus reducing the FoM. The drain current of $M_{1,2}$ transistors has almost a square waveform when the current source is ideal and so $\alpha_I = \frac{2}{\pi}$ (see Figure 2.3(c)). However, in a real scenario, a non-ideal current source will bring up some issues and limitations. First of all, M_T transistor will contribute to the phase noise, thus increasing the noise factor beyond $1 + \gamma$. The minimum tail node voltage, V_T , is also limited by the need to keep the M_T transistor in saturation; consequently the maximum oscillation voltage amplitude reduces to $V_{DD} - V_{sat}$ and so $\alpha_V < 1$ ($\alpha_V \approx 0.8$). The capacitance at node T tends to keep its voltage at a constant level. Consequently, for large oscillation amplitudes with $M_{1,2}$ entering the triode region, the ideal square wave of $M_{1,2}$ drain current experiences a dimple, as shown in Figure 2.3(c). Hence, α_I drops from the ideal value of $\frac{2}{\pi}$, and phase noise is increased. On the other hand, when M_1 or M_2 transistors enter triode region for a portion of oscillation period, they will show a low impedance. Furthermore, the equivalent parasitic capacitance at node T creates a low impedance path to ground. Therefore, the tank finds a discharge path to the ground for the time that either one of these transistors is in the triode region and so its quality factor drops, thus limiting the oscillator's phase noise. The M_T transistor size is usually relatively large in order to reduce its flicker noise. Consequently, the parasitic capacitor at node T is large enough to provide such a low frequency path. However, it is also helpful in partially filtering the M_T transistor's thermal noise.

Various solutions are proposed in the literature to improve the class-B topology phase noise or to improve the oscillator's phase noise-power consumption trade-off by introducing new classes of oscillations. One of the most effective techniques that could improve the class-B considerably is the noise filtering technique [17]. In this technique, the M_T 's thermal noise is filtered by a relatively large capacitor and a high impedance path is inserted between the core transistors and M_T to deny any discharge path to the tank. Although this technique is very effective, since the high impedance path is realized by another resonator, it increases the die area significantly. Another interesting technique to improve the oscillator's phase noise is to couple N oscillator cores together [18]. This technique has been used in microwave circuits [19] and also employed to improve phase noise in RF applications [20]. With coupling N cores, phase noise reduces by a factor of N while the power consumption increases by the same factor. Consequently, although the phase noise is reduced, the FoM remains the same. However, the die area is surely getting N times larger.

In the following sections, we briefly review other oscillator topologies that attempt to improve the phase noise–power consumption trade-off in an oscillator. In a class-C structure, $M_{1,2}$ are biased in a way as to always remain in saturation during the whole oscillation period. In another strategy, the oscillation waveforms in class-D and class-F structures offer special impulse sensitivity functions (ISFs) that prevent circuit noise from upconverting to phase noise.

2.3 Class-C Oscillator Topology

Class-C structure [21] is shown in Figure 2.5(a). In this class of operation, the core transistors are kept in saturation and, consequently, they show a high impedance during the entire oscillation period. The tank does not find a discharge path to the ground and so its quality factor is preserved. This structure also saves 36% of the power consumption for the same phase noise by changing the square pulses of the $M_{1,2}$ drain current in class-B operation to narrow and tall pulses with $\alpha_I = 1$. To ensure the saturation region of operation, $M_{1,2}$ transistor gates are decoupled from the tank's oscillation voltage and are biased at a value well below the V_{DD} voltage. A large



Figure 2.5 (a) A class-C oscillator schematic and (b) its voltage waveforms.

capacitor in parallel with the M_T current source allows class-C like tall and narrow current pulses for the $M_{1,2}$ transistors.

However, the maximum oscillation amplitude is limited in this topology. If the oscillation amplitude gets large enough to push $M_{1,2}$ into triode region, not only the tank's quality factor heavily drops due to large C_T , but also $M_{1,2}$ drain current will no longer be tall and narrow pulses and α_I dramatically drops. Consequently, although the phase noise and power efficiency are improved for low oscillation amplitudes compared to class-B oscillator structure with the same amplitude, the minimum achievable phase noise of this structure is limited. An attempt to increase the class-C swing is done by removing the current source transistor M_T and generating V_{bias} by a current mirror circuit [22]. That oscillator topology also suffers from a tradeoff between its robust start-up and the maximum oscillation voltage in steady state [23]. V_{bias} should be relatively large to facilitate start-up, but large V_{bias} values limit the steady-state oscillation amplitude. It was proposed to adjust V_{bias} dynamically in a negative feedback loop [23-25], which consumes extra power (see Figure 2.6(a)), or to employ class-B switching transistors in parallel with the class-C ones to ensure start-up for low V_{bias} values [26,27], which reduces α_I and consequently power efficiency (see Figure 2.6(b)). The power efficiency of this structure motivated designers in [28] to incorporate this oscillator topology in a Bluetooth low energy (BLE) transmitter.



Figure 2.6 (a) A class-C with dynamic generation of V_{bias} [23]; (b) a hybrid class-B/class-C oscillator [27].

Interestingly, the inherently low flicker noise operation of class-C has long eluded proper explanation. It was only very recently explained in [13] by applying the principles disclosed in this book.

2.4 Class-D Oscillator Topology

The schematic of this oscillator topology is shown in Figure 2.7(a). The tail transistor is removed in this structure, eliminating the overhead voltage necessary for the tail current source transistor. Furthermore, $M_{1,2}$ transistor sizes are chosen large enough to become almost ideal switches. The oscillation voltage amplitude is maximized in this structure and reaches about $3V_{DD}$. By doing so, it pushes $M_{1,2}$ transistors deep into the triode region (even more than in the class-B structure) and, consequently, they generate considerable amount of noise. However, as demonstrated in Figure 2.7(b), the oscillation voltages, V_1 or V_2 , are forced to ground for almost half the period. V_1 (V_2) is mostly grounded when M_1 (M_2) is in the triode region, and, consequently, the ISF of node D_1 (D_2) is almost zero for most of this period, preventing M_1 (M_2) noise to be upconverted to phase noise.

The idea of voltage-switching oscillators was first proposed in 1959 [29] with a discrete BJT implementation, consequently not suitable for RF applications. However, recent CMOS technologies make excellent switches with reasonable sizes available and consequently this structure is attracting an increasing interest [30–32]. The high oscillation amplitude in this structure makes it suitable for low-voltage low-phase-noise applications [32, 33].



Figure 2.7 (a) A class-D oscillator schematic and (b) its voltage waveforms.

The product of the drain current through MOS switches and voltage is almost zero across the oscillation period, consequently the power efficiency of this structure is beyond 90% [31]. However, this oscillator structure not only *can* work with low voltage supplies but it *should* utilize low power supply voltages, otherwise the $M_{1,2}$ transistors, which should be thin-oxide devices to guarantee nearly ideal switching, will face breakdown. Another limitation of the class-D structure is its relatively high upconversion of low-frequency noise as well as high supply pushing. It has been tried to minimize this problem by an on-chip LDO in [34], but it is power consuming. We elaborate this problem in detail in Chapter 5 and then disclose a solution.

2.5 Class-F Oscillator Topologies

If the ISF of a certain oscillation waveform is negligible for some amount of oscillation period, the circuit noise cannot be upconverted to phase noise during that time, which is beneficial in reducing the oscillator's phase noise. Class-F oscillators realize such oscillation waveforms by giving rise to either *third* or *second* harmonic of oscillation voltage [35–39]. This class of oscillators is discussed in detail in Chapters 3 and 4.

2.6 Conclusion

In this chapter, we briefly introduced different oscillator structures and mentioned their benefits and drawbacks. We discussed the nonidealities that the traditional class-B oscillators face and reviewed how each structure tries to overcome them. Class-C oscillators improve phase noise for the same power consumption but only when the oscillation amplitude is low enough to keep the core transistors in saturation. Class-D oscillators offer a very low noise without requiring large supply voltages, but they are limited to low supply voltages due to reliability concerns. Class-F oscillators create waveforms with a special ISF that prevents conversion from the circuit thermal noise to phase noise.

References

- B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, Mar. 1996.
- [2] M. Mikhemar, D. Murphy, A. Mirzaei, and H. Darabi, "A cancellation technique for reciprocal-mixing caused by phase noise and spurs," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3080–3089, Dec. 2013.
- [3] H. Wu, M. Mikhemar, D. Murphy, H. Darabi, and M. F. Chang, "A blocker-tolerant inductor-less wideband receiver with phase and thermal noise cancellation," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2948–3024, Dec. 2013.
- [4] J. Borremans et al., "A 40 nm CMOS 0.4-6 GHz receiver resilient to out of band blockers," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1659–1671, Jul. 2011.
- [5] H. Darabi et al., "A quad band GSM/GPRS/EDGE SoC in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 870–882, Apr. 2011.
- [6] E. J. Baghdady, R. N. Lincoln, and B. D. Nelin, "Short-term frequency stability: Characterization, theory, and measurement," in *Proc. IEEE*, vol. 53, pp. 704–722, Jul. 1965.
- [7] L. S. Cutler and C. L. Searle, "Some aspects of the theory and measurement of frequency fluctuations in frequency standards," in *Proc. IEEE*, vol. 54, pp. 136–154, Feb. 1966.
- [8] D. B. Leeson, "A simple model of feedback oscillator noises spectrum," in *Proc. IEEE*, vol. 54, pp. 329–330, Feb. 1966.
- [9] J. Rutman, "Characterization of phase and frequency instabilities in precision frequency sources; Fifteen years of progress," in *Proc. IEEE*, vol. 66, pp. 1048–1174, Sept. 1978.
- [10] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

- 24 LC Oscillator Structures
- [11] A. Demir, A. Mehrotra, and J. Roychowdhury, "Phase noise in oscillators: a unifying theory and numerical methods for characterization," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 5, pp. 655–674, May 2000.
- [12] D. Murphy, J. J. Rael, and A. A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1187–1203, June 2010.
- [13] Y. Hu, T. Siriburanon, and R. B. Staszewski, "Intuitive understanding of flicker noise reduction via narrowing of conduction angle in voltagebiased oscillators," *IEEE Trans. on Circuits and Systems II (TCAS-II)*, pp. 1–5, 2019.
- [14] A. Hajimiri and T. Lee, "Design issues in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.
- [15] J. Rael and A. Abidi, "Physical processes of phase noise in differential LC oscillators," *in Proc. IEEE Custom Integr. Circuits Conf.*, Sept. 2000, pp. 569–572.
- [16] P. Andreani et al., "A study of phase noise in Colpitts and LCtank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.
- [17] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.
- [18] A. Hajimiri, "Distributed integrated circuits: An alternative approach to high-frequency design," *IEEE Commun. Mag.*, vol. 40, no. 2, pp. 168–173, Feb. 2002.
- [19] H. Chang, X. Cao, U. K. Mishra, and R. A. York, "Phase noise in coupled oscillators: Theory and experiment," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 5, pp. 604–615, May 1997.
- [20] L. Roman, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "5-GHz oscillator array with reduced flicker up-conversion in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2457–2467, Nov. 2006.
- [21] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.
- [22] M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, "High-swing class-C VCO," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2011, pp. 495–498.

- [23] L. Fanori and P. Andreani, "Highly efficient class-C CMOS VCOs, including a comparison with class-B VCOs," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1730–1740, Jul. 2013.
- [24] W. Deng, K. Okada, and A. Matsuzawa, "A feedback class-C VCO with robust startup condition over PVT variations and enhanced oscillation swing," in *IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2011, pp. 499–502.
- [25] J. Chen, F. Jonsson, M. Carlsson, C. Hedenas, and L. R. Zheng, "A low power, start-up ensured and constant amplitude class-C VCO in 0.18 μm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 8, pp. 427–429, Aug. 2011.
- [26] K. Okada, Y. Nomiyana, R. Murakami, and A. Matsuzawa, "A 0.114 mW dual-conduction class-C CMOS VCO with 0.2 V power supply," in *Proc. IEEE Symp. Circuits*, Jun. 2009, pp. 228–229.
- [27] L. Fanori, A. Liscidini, and P. Andreani, "A 6.7-to-9.2 GHz 55 nm CMOS hybrid class-B/class-C cellular TX VCO," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 354–356.
- [28] C. Li and A. Liscidini, "Class-C PA-VCO cell for FSK and GFSK transmitters," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1537–1546, Jul. 2016.
- [29] P. Baxandall, "Transistor sine-wave LC oscillators. Some general considerations and new developments," *Proc. IEE–Part B: Electron. Commun. Eng.*, vol. 106, no. 16, pp. 748–758, May 1959.
- [30] L. Fanori and P. Andreani, "A 2.5-to-3.3 GHz CMOS class-D VCO," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 346–347.
- [31] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.
- [32] A. G. Roy, S. Dey, J. B. Goins, T. S. Fiez, and K. Mayaram, "350 mV, 5 GHz class-D enhanced swing differential and quadrature VCOs in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1833–1447, Aug. 2015.
- [33] Y. Yoshihara, H. Majima, and R. Fujimoto, "A 0.171 mW, 2.4 GHz class-D VCO with dynamic supply voltage control," in *IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2014, pp. 339–342.
- [34] L. Fanori, T. Mattsson, and P. Andreani, "A class-D CMOS DCO with an on-chip LDO," in *IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2014, pp. 335–338.

- 26 LC Oscillator Structures
- [35] H. Kim, S. Ryu, Y. Chung, J. Choi, and B. Kim, "A low phase-noise CMOS VCO with harmonic tuned LC tank," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 7, pp. 2917–2923, Jul. 2006.
- [36] D. Manstretta and R. Castello, "An intuitive analysis of phase noise fundamental limits in LC oscillators", in *International Conference on Noise and Fluctuations (ICNF)*, 2015.
- [37] M. Babaie, and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.
- [38] F. W. Kuo, R. Chen, K. Yen, H. Y. Liao, C. P. Jou, F. L. Hsueh, M. Babaie, and R. B. Staszewski, "A 12 mW all-digital PLL based on class-F DCO for 4G phones in 28 nm CMOS," in *Proceedings of IEEE VLSI Circuits Symposium*, 2014, pp. 1–2.
- [39] M. Babaie and R. B. Staszewski, "An ultra-low phase noise class-F₂ CMOS oscillator with 191 dBc/Hz FOM and long term reliability," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 679–692, Mar. 2015.