Transconductance Enhanced Cross Coupled Dynamic Comparator using 90nm CMOS Technology

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Abstract.

Dynamic Comparators are in demand these days due to many advantages they have Comparator is a part of analog circuit As its name suggests, it compares two values and gives the desired result as required by the user We use dynamic comparators as they use positive feedback which is not used by others It improves the timings and also other specifications like speed It is implemented easily as compared to other designs It revolves around digital standard cells which operates at low voltages There are many types of comparators which have their own advantages over the other designs Kickback noise is the one factor by which a latched comparator suffers also in this type , common-mode kickback noise We can think of other designs and two stage design is used preferably as it has a low disturbance ,lower offset and also this disturbance can be declined by separating the input nodes The circuit was made in Cadence Virtuoso tool by using GPDK (Generic Process Design Kit) 90nm CMOS technology.

Keywords. Dynamic Comparator,Transconductance Comparator,Cadence Virtuoso, latch, transistor, kickback noise.

1. INTRODUCTION

Comparators are one of the digital additives which are broadly used with inside the global Comparators are a one bit analog to virtual converter utilized in ADC converter In the method of changing an analog sign to virtual, the enter is sampled after which implemented to a series of comparators to decide the virtual equal of the analog in sign Comparator reaction time decide the conversion charge Comparator is likewise utilized in a pass detector, top detector, records transfer, switching energy regulator and others Comparator is used to evaluate analog enter in regards sign presents binary equal output primarily based totally at the evaluation Comparators may be divided into kinds relying on structure Static comparators are those who carry out threshold detection primarily based totally on an in and reference without a clock These are easy gadgets with not able as circuit implementations, however do now no longer locate actual use within side the global of excessive velocity records converters So comparators are regularly called Dynamic Comparators Dynamic comparators, on the alternative hand, use a phase/time primarily based totally clock

mechanism to carry out the switching action. The clock speed commonly defines the rate of the comparator and the every day average speed of the ADC. A CMOS dynamic comparator has different components, a preamplifier and, a dynamic latch. The layout of the preamplifier determines the offset voltage.The latch determines the rate of the comparator, if the offset voltage is decreased it at once facilitates enhance accuracy It calls for big enter transistors of the preamplifier-amplifier which will increase parasitic capacitance and as a result energy in take Voltage in not unusual place mode it's far implemented to the enter to perform the enter transistors in saturation which enables to growth,the rate however the version of enter voltage in not unusual place mode outcomes in large put off variability which makes the circuit now no longer appropriate for excessive speed operation There are numerous strategies that have been proposed to date via way of means of one of a kind through the authors to lessen the energy intake, boom the speed and accuracy of the comparator circuit There are strategies that target on enhancing the preamplifier circuit to lessen the offset whilst preserving the latch. Paintings as it's far, enhancing the dynamic latch to enhance pace, offers 0 static energy intake, however the pace is compromised Comparator isn't best utilized in analog to virtual converter, however has different packages In virtual in formation transfer, switching strength regulators and others, the comparator has its very own meaning.

2. CONVENTIONAL DYNAMIC COMPARATOR

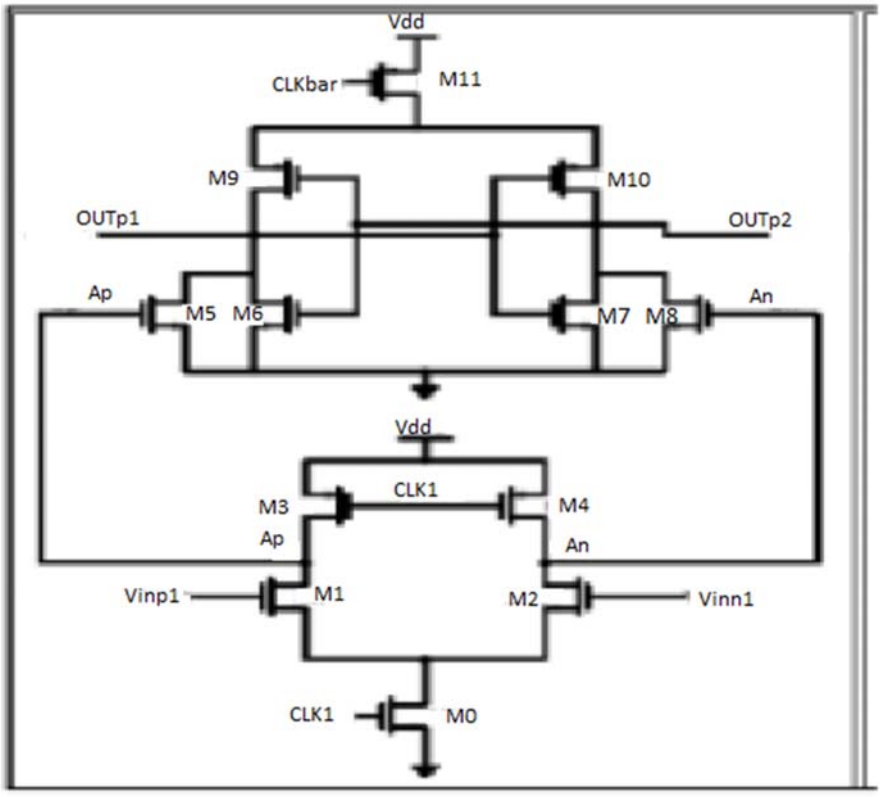

Figure 2.1.Conventional Dynamic Comparator [5]

The standard dynamic comparator is dispensed in given figure. In t represents NMOS type preamplifier and similar diagram can represents PMOS type preamplifier by changing NMOS with PMOS. The operation depends on the clock signal, there are two signals namely CLK and CLKbar to make the circuit operate in two stages, evaluation stage and reset stage. When CLK = 0 i.e CLKbar = 1, the transistors M3 and M4 charge Ap and An node to power supply (VDD) and as M0 is OFF, it in addition to M3 ans M4 makes M5 and M6 ON, thus OUTp1 and OUTp2 nodes are released to ground and hence called reset stage. On the other side when CLK = 1 i.e CLKbar = 0,the difference in signal is boosted by the pre-amplifier at two transistors M1 and M2 respectively, this signal at Ap and An wires is created which then gets boosted further by M6 and M5 and hence called the evaluation stage. The difference thus obtained acts as input for the inverters which are cross coupled and are further converted to power supply (VDD) and ground as there is positive feedback. Now the output of the circuit will come according to the difference in inputs which justifies the operation of a comparator. As discussed earlier there are two stages, in the evaluation stage it does not stop working even after latching of correct value and causes dissipation of power. The clock needs a very high accuracy timing as latch measure needs to preserve the difference in input voltages and thus this acts as a disadvantage of this circuit.

2.1 Cross Coupled Conventional Dynamic Comparator

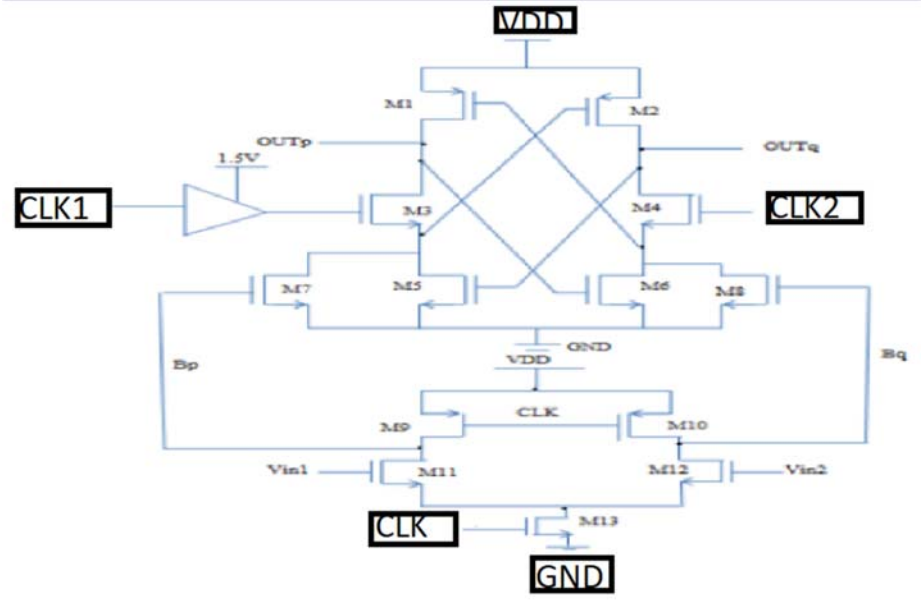

Figure 2.2.Conventional Dynamic Comparator[7]

In this figure, latching level makes use of separately biased gate cross coupled transistors instead of the standard cross-coupled inverter circuit. There are advantages of both as dynamic comparators need positive feedback and low static usage of power and high speed. Standard one stage dynamic comparator have disadvantages as they experience voltage headroom and kickback noise which becomes doubtful as speed and power suffer.:large. Standard two-stage dynamic comparator has advantages like less stacking, appropriate for low-voltage operation and reduced kickback noise which leads to low power usage and hence it is preferred. Improvising the net transconductance is a method to decrease delay and as only PMOS is on it causes low regeneration velocity which leads to increased time in metastable state and inturn leads to higher power consumption .

2.2 Transconductance Enhanced Dynamic Comparator

A dynamic comparator with a fresh latching stage in addition to transconductance is depicted. This stage consists of transistors which are cross coupled as earlier in place of back to back connection of inverters. The frequency was limited earlier as there was constant re designing of pre amplifier but not the latch. The performance depends on the transconductance in the initial phase and if it is large then there will be low dissipation of power and high speed. Now the transistor sizing is also crucial as the same pre amplifier stage is being used which can also lead to high parasitics and can affect the boosting stage. So, we name it transconductance enhanced as it is totally dependent on this value and by further improvements many constraints can be matched.

3. RESULTS AND SIMULATIONS

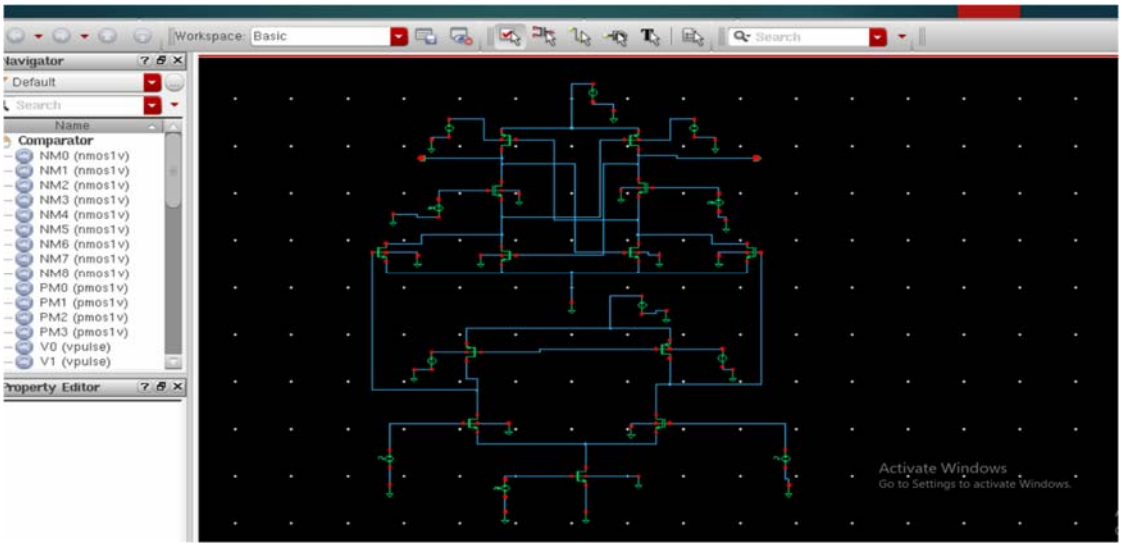

Figure.3.1 Transconductance-Enhanced Dynamic Comparator

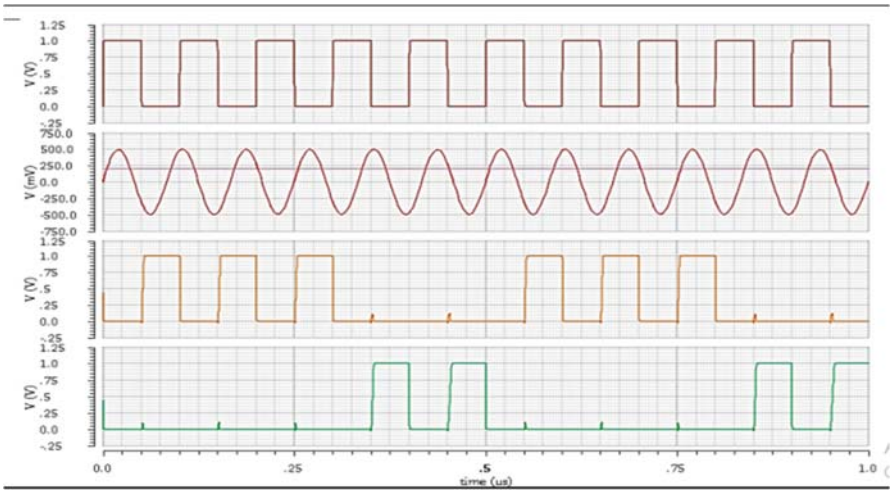

Figure.3.2 Dynamic Comparator Output Waveform

The transient analysis of the transconductance enhanced dynamic comparator circuit is shown above. From this analysis it can be observed that noise affects one of the output nodes in latch as it changes with the transitioning in the clock. For the transient analysis we have taken pulse voltage(vpulse) as input and a dc voltage(vdc) as reference node. Different latching configurations present in the circuit help in increase speed. The delay has been decreased to 228ps when operated at f<2.5GHz. As a modification in latch configuration has

been used it leads to a higher frequency of operation. It also takes up less area than before. If offset voltage is to be reduced to 2mV, the maximum operating frequency drops with a satisfactory delay.

4. CONCLUSION

The tender cross-coupled dynamic comparator has latching level and preamplifier level. In latching level as long as strong positive feedback exists there will be very less power usage. In preamplifier stage there is significant improvement in gain and reduction of unwanted noise . The cross-coupled dynamic comparator has two stages as mentioned earlier, one is reset and other is evaluation or comparison stage. One resets the transistors while the other uses difference in input voltages. In reset phase latching circuit is sway in strong inversion region leading to increase in trans-conductance of the latch. In comparison phase it will tend to decrease delay as well as power usage. The results have been simulated using Cadence Virtuoso in CMOS 90nm technology and it shows improved gain and takes up less area than the standard one.

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Biographies

Harpreet Kaur has done bachelor's degree in electronics and communication engineering from PEC University Of Technology in 2021, pursuing the master's degree in VLSI Design from PEC University Of Technology.

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