Development & Property study of Partially Depleted Silicon-On-Insulator MOSFET

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Abstract

The results of process and device simulation using Silvaco TCAD tools to develop a Partially Depleted Silicon-On-Insulator Metal Oxide Semiconductor Field Effect Transistor (PD SOI MOSFET) are presented in this paper. The purpose of this simulation work is to investigate the drain current and global device temperature variation of the device as the oxide material consisting of the buried oxide layer changes from Silicon dioxide (SiO_2) to Hafnium dioxide (HfO_2) and Zirconium dioxide (ZrO_2). The results also show the energy band diagrams for all three oxide materials. The device is virtually fabricated with ATHENA software, simulated with ATLAS software in the DeckBuild environment, and all graphs are plotted in Silvaco with TonyPlot.

Keywords. Silicon-On-Insulator, MOSFET, Silvaco, ATHENA, ATLAS.

1. INTRODUCTION

The Silicon on Insulator Metal Oxide Semiconductor Field Effect Transistor (SOI-MOSFET) has several distinct properties, including lower parasitic capacitance, protection from electrostatic discharge, minimal short channel effects (SCEs), lower noise, and improved sub-threshold slope, excellent adaptability, improved radiation hardness, minor fringing capacitance, appealing isolation, latch-up security, high velocity, high temperature, and high-recurrence execution. Most of the research works in developing SOI-based integrated circuits benefit from these characteristics (ICs) [1].

Long back ago, J.E Lilienfield patented the first field effect transistor concept, titled "Method and Apparatus for Controlling Electric Currents," which evolved into the modern metal oxide semiconductor field effect transistor, MOSFET. He proposed a three-terminal device in which the source-to-drain current is controlled by a gate field effect and is dielectrically isolated from the rest of the device. The device's active component is made of a thin semiconductor film deposited on an insulator. Coincidentally, the first proposed FET was an SOI device [2]. Partially Depleted SOI device design is easier to manufacture but it requires more sophisticated device and circuit design to mitigate the effects of the floating-body.

Technology Computer-Aided Design (TCAD) is a design and simulation software which acts as a virtual platform for designing, fabricating, and then operating semiconductor devices such as Bipolar Junction Transistor (BJT), Metal Oxide Semiconductor Field Effect Transistor (MOSFET), and so on. This is critical for

understanding and testing the functionality of the designed device structure before proceeding with the real-time fabrication process and aids in the extraction of device parameters by studying the device's simulated characteristics.

DeckBuild is SILVACO's virtual platform-based wafer fabrication program's front-end Graphical User Interface (GUI). The framework of this program connects a wide range of process and device simulation tools available through SILVACO and allows them to work in an organized, glitch-free, and efficient manner. DeckBuild's pull-down menus aid in syntax creation and provide basic simulation controls. ATLAS and ATHENA are frameworks for multidimensional device simulation. As a result, the SOI MOSFETs can be generated in the ATHENA simulation environment using its layout-based simulation syntax, and ATLAS is used to solve the device's outputs [3].

ATHENA can simulate physical etching, shallow implant, RTA diffusion process stages, and local oxidation to create silicon islands. Among standard models for BULK and SOI technologies, ATLAS offers the following features for SOI-specific device simulation: Self-heating model for modelling of negative differential resistance, impact ionisation model for breakdown and kink effect [4].

The version of Silvaco DeckBuild used to write the code is 5.2.14.R. Version 5.2.3.R Silvaco TonyPlot is used to show the resulting device and graphs.

2. MATERIALS

In this paper, the main focus are three materials: SiO_2, HfO_2 and ZrO_2.

Silicon dioxide (SiO_2) films on silicon serve as the foundation for metal-oxide semiconductor (MOS) field-effect transistors (FET), which are at the heart of the majority of today's very-large-scale integrated (VLSI) circuits. The study and understanding of the properties of these films, as well as the physics of SiO_2, are thus critical to the semiconductor industry [5].

The main reasons for using SiO_2 are its excellent insulating properties of at low and medium electric fields, as well as the development of SiO_2 is relatively simple and via inexpensive growth techniques.

Oxygen-ion ($^{16}O^+$) implantation into silicon produced buried SiO_2 layers. Watanabe and Tooi [6] were the first to report the formation of SiO_2 layers in silicon via oxygen-ion implantation.

HfO_2 has a high melting temperature, low thermal conductivity, and a high dielectric constant (relative to SiO_2 and other gate dielectrics). HfO_2 was investigated as a high-k gate dielectric due to its higher dielectric permittivity than that of SiO_2. Because of its high melting temperature and low thermal conductivity, hafnium dioxide (HfO_2) has long been used as a refractory material [7].

With its excellent chemical and physical properties, zirconium oxide (ZrO_2), also known as zirconia, has applications such as fuel cells, gas sensors, optoelectronics, catalysts, and corrosion resistant materials. ZrO_2 is an important luminescent material with good optical transparency and a potential candidate for photocatalytic applications

due to its high surface area and presence of a large number of oxygen vacancies, with a band gap of >5 eV [8].

The material properties for HfO_2 and ZrO_2 considered for this paper is shown in Table: I.

TABLE: I TABLE OF MATERIAL PROPERTIES [9][10][11]

Material	**Material Properties**					
	Permittivity	***Thermal Conductivity (W/mK)***	***Affinity***	***Band Gap (eV)***	***Conduction Band Density***	***Valence Band Density***
HfO_2	25	1	2	5.9	75	150
ZrO_2	29	2	1.64	5.8	11	15

TABLE: II TABLE OF IMPLANT MOMENTS [13]

Material	**Impurity**	**Impurity Concentration** (ions/cm^2)	**Energy (keV)**	**Implant Moment Data**			
				Range (Micron)	***Std. Dev (Micron)***	***Gamma***	***Kurtosis***
HfO_2	Boron	8.0e12	100	0.2171	0.075	-0.0154	2.3748
		9.5e11	10	0.0252	0.075	0.5152	2.8775
	Phosphor	3.0e13	20	0.0198	0.075	0.6216	3.1655
	Arsenic	5.0e15	50	0.0243	0.075	0.5738	3.1171
ZrO_2	Boron	8.0e12	100	0.3081	0.075	-0.3166	2.6510
		9.5e11	10	0.0416	0.075	0.3669	2.6613
	Phosphor	3.0e13	20	0.0294	0.075	0.4814	2.9370
	Arsenic	5.0e15	50	0.0344	0.075	0.4193	2.9775

The data of table: II is found from the software SRIM version SRIM-2008.04. Moments define the tables and spatial moments that are employed within the analytical implant models.

The predicted range is specified by RANGE (RP); the units are in microns. The standard deviation is specified by STD.DEV, and the units are in microns. The third and fourth moments are specified by Gamma (skewness) and Kurtosis respectively [12].

3. VIRTUAL FABRICATION PROCESS OF SOI MOSFET USING ATHENA SIMULATOR

For the base model, The SOI MOSFETs used in this study were made on p-type (100) UNIBOND SOI wafers with a buried oxide of 1 micron. ATHENA (Silvaco) and ATLAS (Silvaco) were used to simulate the process conditions and two-dimensional (2-D) device characteristics, respectively. Boron-ion implantation was performed on 100 pears to introduce an impurity into the channel region. The top silicon layer was then thermally oxidised to a thickness of 0.03 micron. The gate oxide layer is formed through diffusion with dry oxygen. A 0.2 micron thick layer of polysilicon layer is deposited. Now, a photolithography step followed by vertical etching, defines the length of the transistor gate contact. Following the formation of the gate oxide layer, the gate is formed. The polysilicon layer is deposited using conformal deposition and etched until it is half the length of the desired gate. Prior to performing polysilicon doping, oxidation will be performed using Fermi method. Due to non-planar 2-D polysilicon structure, the compress method is used. Following polysilicon oxidation, the polysilicon is doped with phosphorus to form an n+ polysilicon gate. The source/drain junction formed by doping arsenic. The arsenic dose staying constant, but the doping energy varies with the thickness of the SOI layer to achieve the same doping concentration for all structures. Before depositing the metal layer, a high dose (5e15 ions/cm2) of arsenic is implanted with 50 pears to build the low resistance of the source and drain regions. A portion of the gate oxide layer is etched to open a contact window for the metal. The metal-S/D contact will then be deposited and etched, leaving only the metal-S/D contact. [14].

Finally, the SOI MOSFET is contacted (from left to right: source, gate, drain) and the electrical behavior of the device is examined. The half structure is then mirrored to produce the full structure. The gate, source, and drain terminals are all defined. There will also be a command to define a flat electrode on the simulation structure's bottom that will serve as the body terminal.

For other test models in the buried oxide layer, HfO_2 and ZrO_2 are used instead of SiO_2. Implant moment data given in Table: I for both HfO_2 and ZrO_2 are used for the implantation of previously mentioned boron, arsenic, and phosphorus dosage.

4. RESULTS & DISCUSSION

The figure 1 shows the SOI MOSFET devices fabricated using Athena. The main difference as this paper focuses on is the buried oxide layer. First device in Figure 1 has SiO_2 (blue

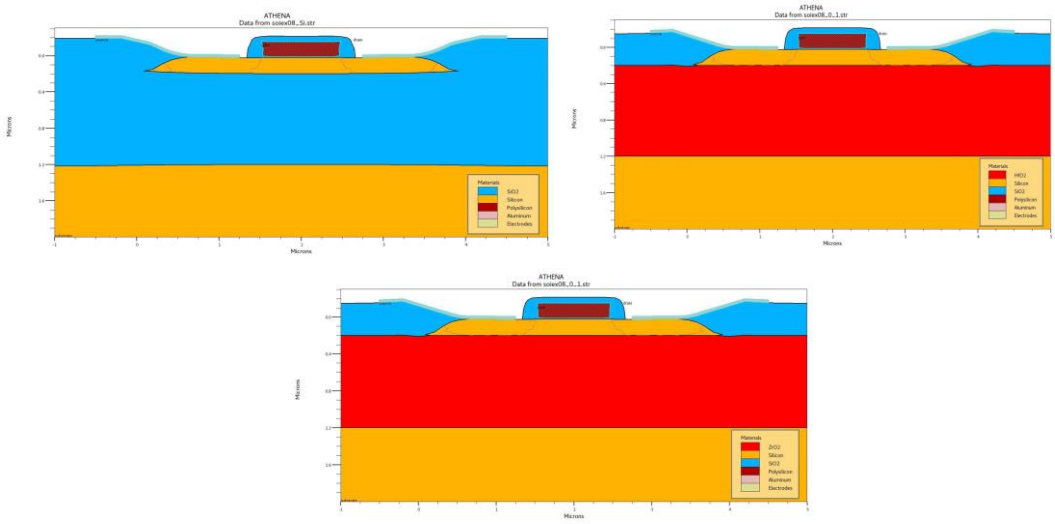

Figure 1: PD-SOI MOSFETs Using SiO_2, HfO_2 and ZrO_2 as buried oxide material

region) as the buried oxide. Second device contains HfO_2 and the last device contains ZrO_2 (red region).

Figure 2 displays all three devices with their net doping concentration. Net doping concentration p0=(N_A-N_D), where N_D represents the net n-type dopant concentration on the n-side and N_A represents the net p-type dopant concentration on the p-side.

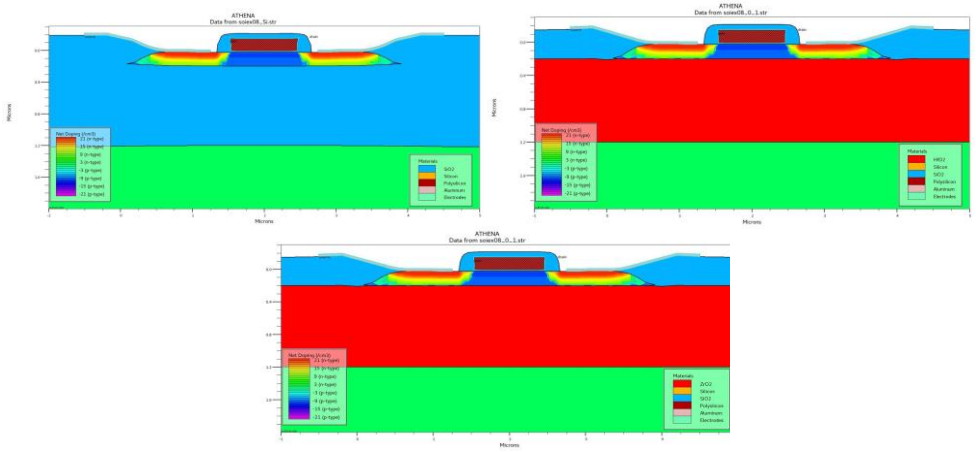

Figure 2: Net Doping Concentration of PD-SOI MOSFETs Using SiO_2, HfO_2 and ZrO_2 as buried oxide material

The newton approach defined in the method statement was chosen as the numerical algorithm for this system of equations. The semiconductor equations are also defined using this statement. carr=2 will solve the potential equation as well as the hole and electron continuity equations.

At each of these bias conditions, the gate voltage is ramped to 0.5, 1, 3, and 5 V and a solution is saved. Using the load command, each solution is then used as the initial starting point for simulating the Ids/Vds characteristics. The terminal characteristics are

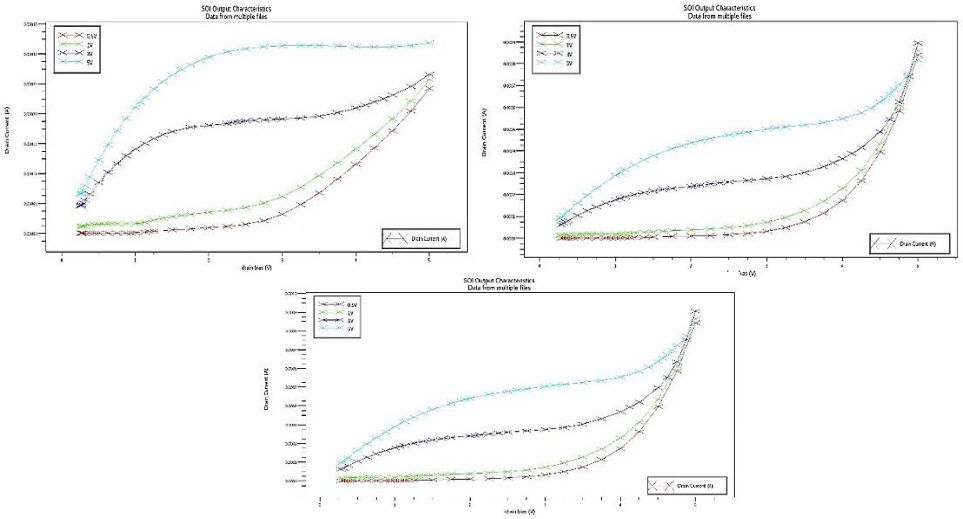

Figure 3: Drain Bias VS Drain Current Graph of PD-SOI MOSFETs Using SiO_2, HfO and ZrO as buried oxide material

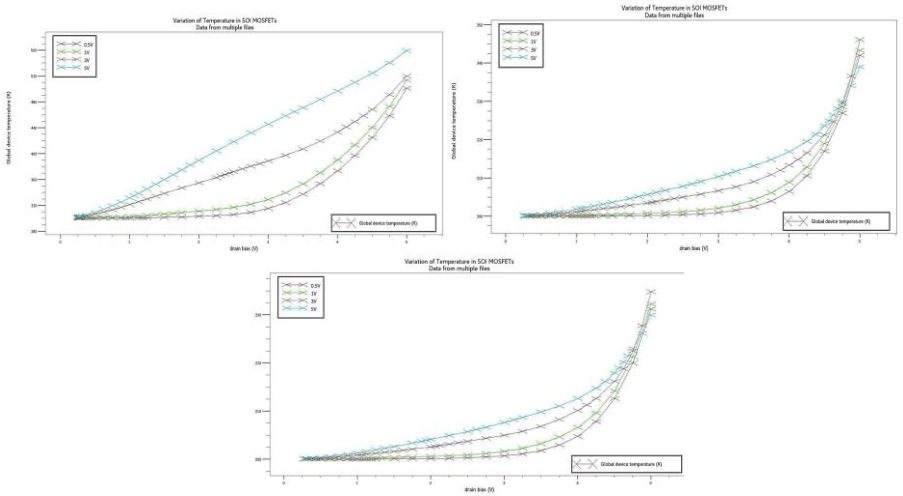

Figure 4: Drain Bias VS Global Temperature Graph of PD-SOI MOSFETs Using SiO_2, HfO_2 and ZrO_2 as buried oxide material

then saved in a logfile, and the drain bias sweep is applied using a solve statement. After that, the procedure is repeated for each gate voltage.

Figure 3 shows the variation in drain current for the same drain bias given for all three devices. Vg (gate voltage) is taken as 0.5V, 1V, 3V and 5V.

Figure 4 is the output of plotting global temperature variation for the same drain bias profile which was taken for Figure 3 which shows less temperature to be generated for the High-K Dielectric materials compared to SiO_2 for the same drain bias.

Figure 5 shows the lattice temperature of the 3 devices. The hcte.el parameter in the DeckBuild code specifies the electron energy balance equation, as well as the lattice heat flow formula is solved with Giga framework by establishing the parameter

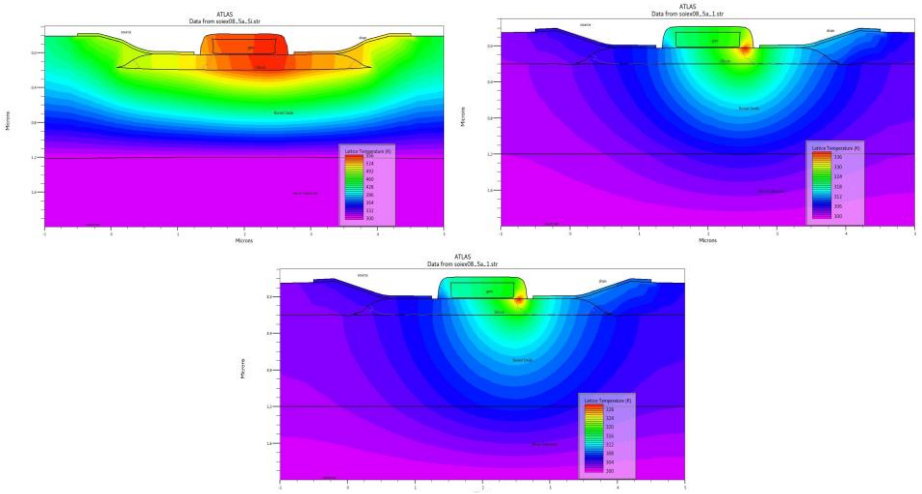

Figure 5: Lattice Temperature of PD-SOI MOSFETs Using SiO_2, HfO_2 and ZrO_2 as buried oxide material

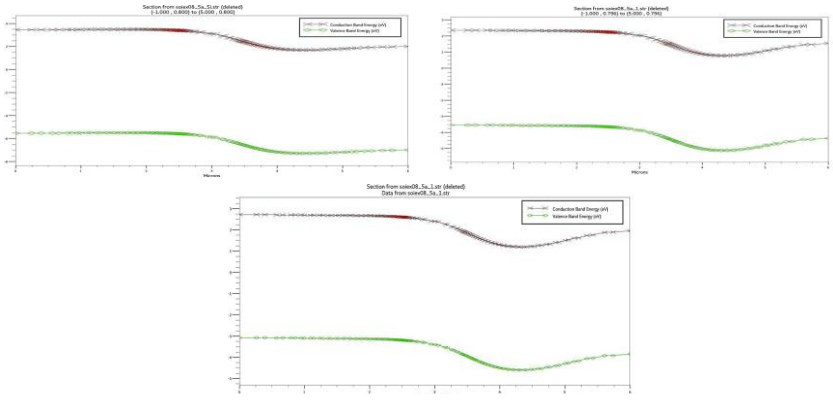

Figure 6: Energy band diagram of PD-SOI MOSFETs Using SiO_2, HfO_2 and ZrO_2 as buried oxide material

lat.temp. Improvement can be seen in terms of lessening the area affected by high lattice temperature in the devices where HfO_2 and ZrO_2 are used instead of SiO_2.

Figure 6 displays band bending of conduction band and valence band for all three devices. The parameters val.band, con.band and band.param are used to get the energy band diagram.

5. CONCLUSION

This paper observes how a PD-SOI MOSFET is fabricated using SILVACO TCAD. It also observes the device structure, net doping concentration and lattice temperature due to changing the buried oxide layer from SiO_2 to high-k dielectric materials such as HfO_2 and ZrO_2 can bring changes to the device. Device characteristics such as the variation in drain current and global temperature with drain bias and band diagram is shown here. The observations show how high-k dielectric materials can improve semiconductor device characteristics and give better results compared to materials such as SiO_2.

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7. REFERENCES

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