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Structured Accelerator Design: Patterns for High-Level Synthesis

Author: Mohammad Hosseinabady, PhD, Computing Consultant, Bristol, UK

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Description:

Accelerators now play a crucial role in computing systems. With the emergence of a new wave of academic and industrial high-level synthesis (HLS) tools, FPGA-based accelerators now are more accessible to software programmers. However, there are several burdens placed upon the programmers to design a high-performance accelerator when using FPGA, such as different memory and parallel programming models. Therefore, a high-level structured design approach targeting accelerator is essential. This approach advances software programming techniques to utilise FPGAs efficiently.

This book explains the concept of accelerator design using current high-level synthesis tools and techniques. It describes different types of regular and irregular accelerator patterns as a structured building block for FPGA implementation. The cutting-edge programming models based on C/C++ and OpenCL are used to explain standard computation and memory patterns through many examples and case studies. In short, this book

- offers theory and practice of HLS parallel programming techniques for FPGA
- describes parallel patterns for regular and irregular algorithms
- contains detailed examples in C/C++ and OpenCL for HLS
- represents the efficiency of FPGA accelerators through several case studies in scientific computation and machine learning areas

Keywords: High-Level Synthesis; FPGA; Parallel Programming Patterns; Hardware Accelerators; Embedded Systems

Denmark Head Office

Alsbjergvej 10
9260 Gistrup
Denmark
www.riverpublishers.com
Email: info@riverpublishers.com

USA Office

Indianapolis, IN
USA
Tel.: +1-3176899634
Email: rajeev.prasad@riverpublishers.com

UK Office

River Publishers
Email: philippa.jefferies@riverpublishers.com