Enhancement of PQ Using Adaptive Theory based Improved Linear Tracer Sinusoidal Control Strategy for DVR

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Abstract

This paper presents the Adaptive Theory based Improved Linear Tracer Sinusoidal (ATILS) Control Strategy for PQ Enhancement using DVR in the Distribution System. The proposed DVR effectively mitigates voltage sag/swell, unbalanced voltage sag/swell for linear loads along with harmonic compensation using ATILS Control Strategy. The DVR consists of voltage source converter (VSC), transformer with capacitor. The main advantages are more efficiency, reliability and its effective control of reactive power. The ATILS Control Strategy is used for extraction of fundamental reference load voltages quickly and accurately to mitigate PQ problems. The proposed ATILS Control Strategy for DVR is modeled using RT-LAB and MATLAB/SIMULINK and its performance is verified for various Power Quality (PQ) problems.

Keywords: DVR, ATILS Control Strategy, Power Quality, Harmonics, Voltage sag/swell.

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1 Introduction

The power quality of available supply has direct economic impact on domestic and manufacturing industries which effects the growth of the nation. This is mainly due to increasing usage of power electronics equipment in day to day life [1]. The reactive power demand and level of harmonic components are popular parameters to specify the reactive power demand at particular load and degree of distortion [2, 3]. In the low and medium power level distribution system, the most commonly occurring problems are related harmonic resonance and Power Quality (PQ). Various standards are proposed by IEEE and IEC to limit power quality problems such as IEEE 519-1992, IEEE Std. 141-1993 and IEC 1000-3-2 etc. [4–6]. The CPDs (Custom Power Devices) are used to mitigate reduction of voltage flicker, harmonic compensation, voltage sag/swell, compensation and resonance due to distortion etc. [7]. It includes DVR (Dynamic Voltage Restorer), DSTATCOM (Distribution Static Compensator) and UPQC (Unified Power Quality Conditioner) in the different configurations [8–10]. The dynamic performance of CPDs depends upon control strategy used for reference load voltage estimation and pulse generation gating scheme.

PQ problems such as voltage sag, swell, unbalance voltage sag/swell, harmonics create severe problems for present modern industry and these problems are compensated using DVR [11]. The three-leg VSC (voltage source converter), transformer with capacitor are the main components of DVR. The major advantage of proposed capacitor based DVR is that it is more efficient and reduces the cost when compared to conventional battery based DVR. Regular maintenance is required for battery based DVR and it adds additional cost for battery. The capacitor based DVR absorbs/injects active power to pre-sag/swell compensation in the distribution system [12, 13].

The design, protection and different topologies for capacitor based DVR are reported in literature [14–16]. To mitigate PQ problems the DVR has to respond quickly for extraction of reference load voltages. A few of the many control strategies for DVR are ISCT (Instantaneous Symmetrical Components Theory) [17], SRFT (Synchronous Reference Frame Theory) [18, 19], Adaline Based Control Algorithm [20], PQR Instantaneous Power Theory [21], Control Algorithm based on Space vector PWM [22], Adaptive Theory based Improved Linear Sinusoidal Control Algorithm for DSTATCOM [23] etc. SRF theory and PQ theory requires reasonable transformations and computations which takes more execution time. Adaline Algorithm requires convergence factor value is so selected to make a tradeoff between the accuracy and the rate

of convergence. ISCT Algorithm applied for DVR then it will show more oscillation the results. All these conventional control strategies take more time for extraction of reference load voltages. The DVR performance is mainly due to effective estimation of reference load voltages with proper control strategy. This paper discusses ATILS control strategy for DVR to mitigate voltage sag/swell for linear/non-linear loads, unbalanced voltage sag/swell. The proposed ATILS control strategy takes less execution time compared to conventional control strategies for generating reference load voltages [24, 25]. The ATILS based DVR is modeled using RT-LAB and MATLAB/SIMULINK and its performance results are validated at different PQ problems.

2 DVR Configuration and Control Algorithm

The ATILS Control Strategy based DVR for generating reference load voltages is shown in Figure 1 along with distribution system. In this proposed control strategy, the phase source voltages (v_{sa}, v_{sb}, v_{sc}), load voltages (v_{La}, v_{Lb}, v_{Lc}), phase source currents (i_{sa}, i_{sb}, i_{sc}), load currents (i_{La}, i_{Lb}, i_{Lc}), dc bus voltage (v_{dc}) and terminal PCC voltages (v_t) are used for estimation of load reference voltages (v_{La}*, v_{Lb}*, v_{Lc}*) based on adaptive theory based improved linear tracer sinusoidal control strategy. In the proposed ATILS Control Strategy based DVR, source currents (i_{sa}, i_{sb}, i_{sc}) are equal to load currents (i_{La}, i_{Lb}, i_{Lc}). To mitigate ripple currents, three inductors (L_f) are used at the VSC and a three phase resistor (R_f) & capacitor (C_f) are connected at the DVR injecting transformer to mitigate voltage harmonics.

2.1 Generation of In-phase and Quadrature Unit Templates

The three-phase instantaneous source currents (i_{sa}, i_{sb}, i_{sc}) may consist of negative sequence components and harmonics. These three phase source currents are given to band pass filters to filter harmonics and noise. The three phase source currents are represented as.

$$i_{sa} = i_{mp} \sin(wt) \tag{1}$$

$$i_{sb} = i_{mp} \sin(wt - {}^{2\pi}/_{3}) \tag{2}$$

$$i_{sc} = i_{mp} \sin(wt - {}^{4\pi}/_{3}) \tag{3}$$

The individual magnitude of each of the three phase source currents (i_{sa}, i_{sb}, i_{sc}) are determined by squaring source currents and estimated currents ($i_{ta}{}^{1}$, $i_{tb}{}^{1}$, $i_{tc}{}^{1}$) are

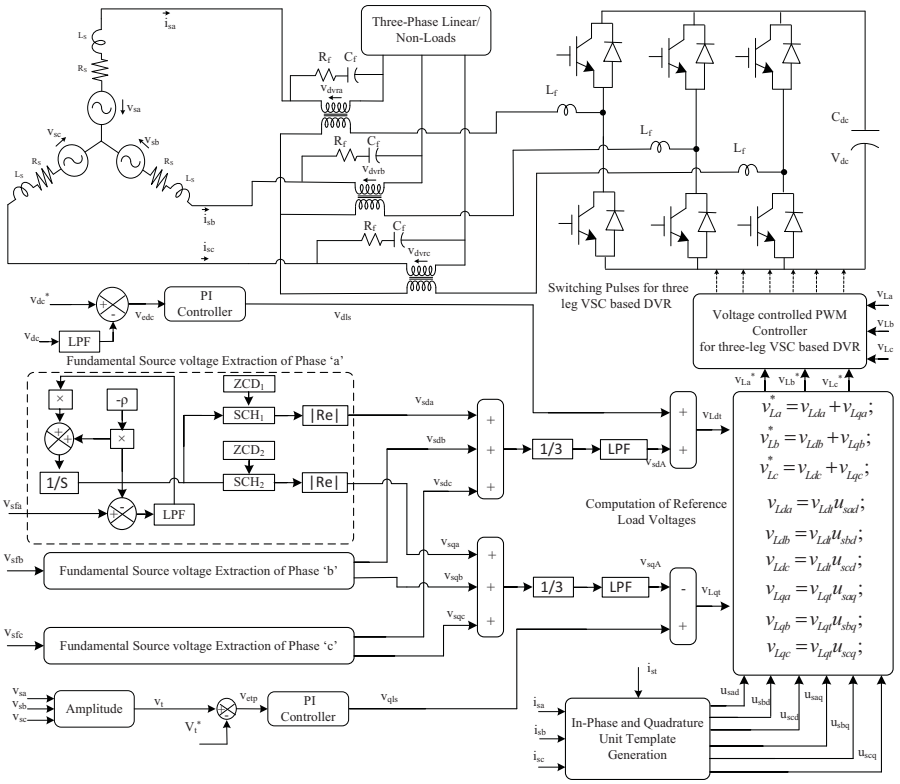

Figure 1 ATILS Control Strategy for three-leg VSC Based DVR in the Distribution System.

$$i_{ta}^{1} = \left[2(i_{sa}^{2})\right]; \quad i_{tb}^{1} = \left[2(i_{sb}^{2})\right]; \quad i_{tc}^{1} = \left[2(i_{sc}^{2})\right]; \tag{4}$$

The total resultant amplitude (i_{st}) of source currents is estimated from source current (i_{ta}^{1}, i_{tb}^{1}, i_{tc}^{1}) and is given as

$$i_{st} = \sqrt{\frac{\left(i_{ta}^{1} + i_{tb}^{1} + i_{tc}^{1}\right)}{3}} \tag{5}$$

In-phase unit-templates (u_{sap}, u_{sbp}, u_{scp}) of three phase source currents are represented as

$$u_{sap} = {}^{i_{sa}}/_{i_{st}}; \quad u_{sbp} = {}^{i_{sb}}/_{i_{st}}; \quad u_{scp} = {}^{i_{sc}}/_{i_{st}}; \tag{6}$$

The quadrature unit-templates (u_{saq}, u_{sbq}, u_{scq}) of three phase source currents are represented as

$$u_{saq} = (-u_{sbp} + u_{scp}) \Big/ \sqrt{3} \tag{7}$$

$$u_{sbq} = (3u_{sap} + u_{sbp} - u_{sbp}) \Big/ 2\sqrt{3} \tag{8}$$

$$u_{scq} = (-3u_{sap} + u_{sbp} - u_{sbp}) \Big/ 2\sqrt{3} \tag{9}$$

2.2 Generation of Fundamental Active and Reactive Power Components of Load Voltages

The proposed adaptive theory based improved linear tracer sinusoidal control strategy is used to estimate fundamental active and reactive power components of load voltages of each phase as shown in the Figure 1. In the fundamental source voltage, phase 'a' component is the difference from the source voltage to estimate the error voltage signal. The filter output of the voltage signal is the combination of output voltage signal with band pass filter (ψ) and this is multiplied with power frequency signal ($-\rho$). The output of this signal is integrated to estimate phase 'a' fundamental source voltage (V_{sfa}). Similarly other two phases 'b' and 'c' fundamental source voltages (V_{sfb} and V_{sfc}) are estimated.

The magnitude of three phase fundamental source voltage active components (v_{sda}, v_{sdb}, v_{sdc}) are extracted at positive zero crossing of in-phase unit templates. The output of ZCD_1 (Zero Crossing Detector) works as trigger pulse for SHC_1 (Sample and Hold Circuit) and fundamental voltage as a input signal of SHC_1. The magnitude of fundamental active component is considered as output of SHC_1 real component. The average magnitude of fundamental source voltage corresponding to active power component (V_{sdA}) is the sum of three phase fundamental source voltage active power components (v_{sda},v_{sdb},v_{sdc}) divided by 3.

$$v_{sdA} = \frac{v_{sda} + v_{sdb} + v_{sdc}}{3} \tag{10}$$

Similarly, the magnitude of three phase fundamental source voltage reactive power components (v_{sqa}, v_{sqb}, v_{sqc}) are extracted at positive zero crossing of quadrature-phase unit templates. The output of ZCD_2 (Zero Crossing Detector) works as trigger pulse for SHC_2 (Sample and Hold Circuit) and fundamental voltage as an input signal of SHC_2. The magnitude of fundamental reactive component is considered as output of SHC_2 reactive component. The average magnitude of fundamental source voltage corresponding to reactive power component (V_{sqA}) is the sum of three phase

fundamental source voltage reactive power components (v_{sqa}, v_{sqb}, v_{sqc}) divided by 3.

$$v_{sqA} = \frac{v_{sqa} + v_{sqb} + v_{sqc}}{3} \tag{11}$$

2.3 Stability Analysis of ATILS Control Strategy

The stability analysis of ATILS Control Strategy is shown in Figure 1. The transfer function gain of low pass filter (G(s)) is as

$$G(s) = 1/\left(1 + s\tau\right) \tag{12}$$

Where τ is the LPF time constant and considered as greater than zero.

The transfer function of phase 'a' is the extracted fundamental source voltage (v_{sfa}) and source voltage (v_{sa}) can be represented as

$$C(s) = \frac{G(s)}{H(s)} = \frac{v_{sfa}}{v_{sa}} \tag{13}$$

Where forward gain is $G(s) = \Psi/(\tau s^2 + (\tau\rho + 1)s + (\psi + \rho))$ and feedback gain of transfer function is H (s) = 1.

The transfer function characteristic equation can be represented as

$$\tau s^2 + (\tau\rho + 1)s + (\Psi + \rho) = 0 \tag{14}$$

Where ψ is the band pass filter frequency, ρ is the power frequency and τ is the LPF time constant. Routh–Hurwitz criterion is used to analyze the stability of the Equation (14).

Routh–Hurwitz criterion array formation is shown in Table 1.

For the stability analysis of ATILS Control Strategy assume band pass filter frequency (ψ) = 250 rad/sec, power frequency (ρ) = 314.14 rad/sec and time constant (τ) = 0.1 sec. By substituting these values in Table 1, it was observed that there is no sign of changes in the first column of Routh–Hurwitz criterion and the characteristic roots are not positive real number. This concludes that ATILS control strategy is stable at different variations in the parameters.

Table 1 Routh–Hurwitz criterion Table

S^2	τ	$\Psi + \rho$
S^1	$\tau\rho + 1$	0
S^0	$\Psi + \rho$	–

2.4 Magnitude of Active Power Voltage Components of Reference Load Voltages

The sensed DC bus voltage ($V_{dc} = (2\sqrt{2}\ V_{LL})/(\sqrt{3}\ m)$ and reference DC bus voltage (v_{dc}^*) of VSC (Voltage Source Converter) are compared and dc bus voltage error at m^{th} sample instant is estimated as,

$$v_{edc(m)} = -v_{dc(m)} + v^*_{dc(m)} \tag{15}$$

The output error of dc bus (v_{edc}) is feeding to PI (Proportional Integral) controller and this output is required to regulate dc bus voltage of DVR at m^{th} sample instant given as

$$v_{dls(m)} = v_{dls(m-1)} + K_{p1}(v_{edc(m)} - v_{edc(m-1)}) + K_{i1}v_{edc(m)} \tag{16}$$

Where $v_{edc}(m)$ and $v_{edc}(m-1)$ are the error in the DC bus voltage at m^{th} and $(m-1)^{th}$ sample instants and K_{p1} and K_{i1} are proportional and integral gain constants.

The magnitude of active power component reference load voltage (V_{Ldt}) is the sum of average magnitude of source voltage component (V_{sdA}) and the DC bus PI controller output (v_{dls}).

$$v_{Ldt} = v_{sdA} + v_{dls} \tag{17}$$

2.5 Magnitude of Active Power Voltage Components of Reference Load Voltages

The sensed load voltage (v_t) and reference load voltage (v_t^*) are compared and error at m^{th} sample instant is estimated as

$$v_{etp(m)} = -v_{t(m)} + v^*_{t\,(m)} \tag{18}$$

The output of error (v_{etp}) is feeding to PI (Proportional Integral) controller and this output (v_{qls}) is required to regulate terminal load voltage of DVR at m^{th} sample instant given as

$$v_{qls(m)} = v_{qls(m-1)} + K_{p2}(v_{etp(m)} - v_{etp(m-1)}) + K_{i2}v_{etp(m)} \tag{19}$$

Where $v_{etp}(m)$ and $v_{etp}(m-1)$ are the error in the load voltage PI at m^{th} and $(m-1)^{th}$ sample instants and K_{p2} and K_{i2} are proportional and integral gain constants.

The magnitude of the reactive power component of load voltage (V_{Lqt}) is the sum of average magnitude of source voltage component (V_{sqA}) and the DC bus PI controller output (v_{qls})

$$v_{Lqt} = -v_{sdA} + v_{qls} \tag{20}$$

2.6 Estimation of Reference Load Voltages and Switching Pulses Generation

The reference load active and reactive components of three phase voltages are estimated by using magnitude of active and reactive component of three phase load voltages using in-phase unit and quadrature unit templates

$$v_{Lda} = v_{Ldt}u_{sad}; \quad v_{Ldb} = v_{Ldt}u_{sbd}; \quad v_{Ldc} = v_{Ldt}u_{scd} \tag{21}$$

$$v_{Lqa} = v_{Lqt}u_{saq}; \quad v_{Lqb} = v_{Lqt}u_{sbq}; \quad v_{Lqc} = v_{Lqt}u_{scq} \tag{22}$$

The reference load voltages (v_{La}^*, v_{Lb}^*, v_{Lc}^*) are estimated using the sum of reference active and reactive power voltage components as

$$v_{La}^* = v_{Lda} + v_{Lqa}; \quad v_{Lb}^* = v_{Ldb} + v_{Lqb}; \quad v_{Lc}^* = v_{Ldc} + v_{Lqc}; \tag{23}$$

These three phase reference load voltages (v_{La}^*, v_{Lb}^*, v_{Lc}^*) are compared with actual load voltages (v_{La}, v_{Lb}, v_{Lc}) and error of the output is compared with triangular carrier wave with 10 kHz frequency for generation of switching pulses DVR.

3 Simulation Results and Discussion

MATLAB/SIMULINK and SPS (Sim power Sytems) toolbox is used for the development of Simulink model of DVR and proposed control strategy. The performance analysis of ATILS control strategy in the time domain and DVR is simulated for voltage sag/swell for linear/non-linear loads and unbalanced voltage sag/swell using simulink model. The performance of ATILS control strategy based DVR is observed for various time varying linear/non-linear loads.

3.1 Performance of DVR based on ATILS Control Strategy in the Voltage Sag Operation During Linear/Non-Linear Loads

The performance of three-leg VSC based DVR on ATILS control strategy during voltage sag at linear/non-linear load is depicted in Figure 2

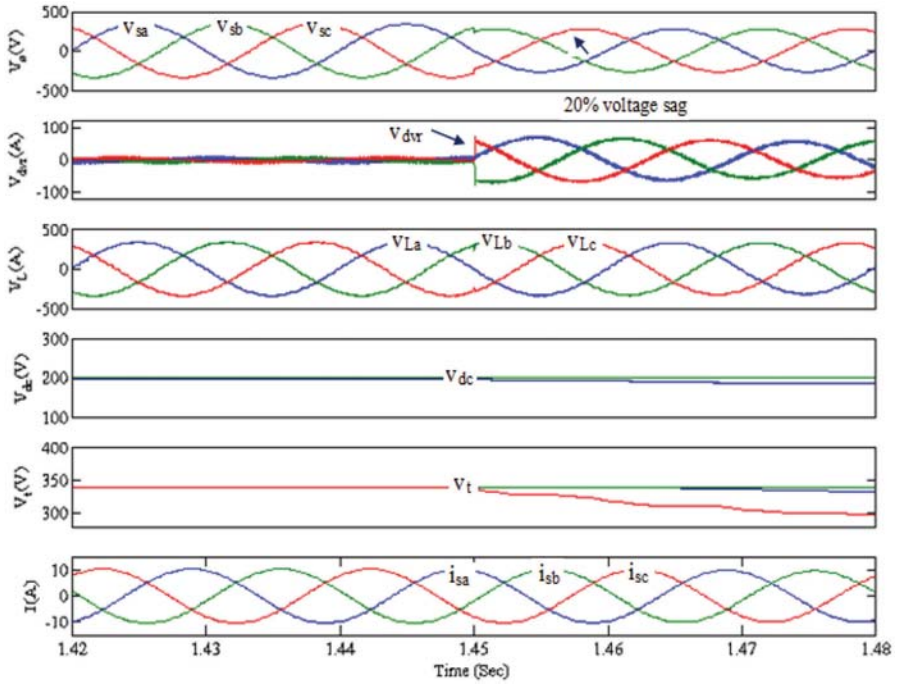

Figure 2 Performance of ATILS Control Strategy based DVR for 20% voltage sag.

and Figure 3. The parameters of performance indices such as supply voltage (v_s), compensating voltage (v_{dvr}), load voltage (v_L), dc bus voltage (v_{dc}), terminal voltage (v_t), load current (i_L) at (t = 1.42 sec to 1.48 sec) linear/non-linear loads are depicted in Figure 2–Figure 3. At t = 1.42 sec the source voltage (v_s), load current (i_L) and load voltage (v_L) are balanced and sinusoidal under linear loads as observed from Figure 2 and Figure 3. A 20% of voltage sag is introduced under linear loads and non-linear load at t = 1.45 sec to 1.48 sec. The proposed ATILS Control Strategy based DVR introduces mitigating voltage in such a manner that the load voltage (v_L) and load voltage (i_L) are sinusoidal and balanced, it was observed that from Figure 2–Figure 3. The actual dc bus voltage (v_{dc}) and its terminal voltage (v_t) of DVR are regulated to rated values at 200 V and 339 V as shown under linear/non-linear loads. The proposed ATILS control strategy based DVR in Figure 2–Figure 3 from t = 1.42 sec to 1.48 sec the performance parameters shows satisfactory results at voltage sag under linear/non-linear loads as per IEC and IEEE standards.

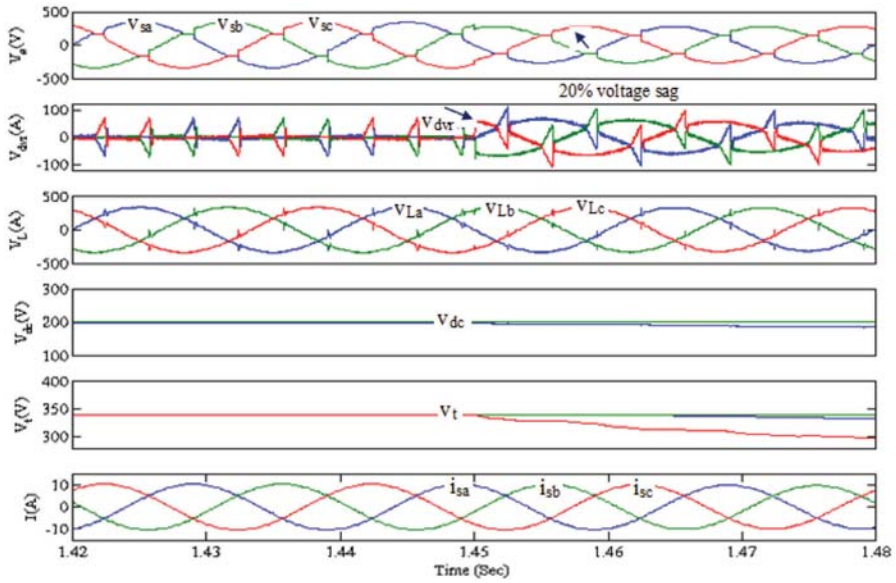

Figure 3 Performance of ATILS Control Strategy based DVR for 20% voltage sag under non-linear loads.

3.2 Performance of DVR based on ATILS Control Strategy in the Voltage Swell Operation During Linear/Non-Linear Loads

The dynamic performance of three-leg VSC based DVR on ATILS control strategy during voltage swell at linear/non-linear load is depicted in Figure 4 and Figure 5. The parameters of performance indices such as supply voltage (v_s), compensating voltage (v_{dvr}), load voltage (v_L), dc bus voltage (v_{dc}), load terminal voltage (v_t), load current (i_L) at (t = 1.42 sec to 1.48 sec) linear/non-linear loads are depicted in Figure 4 and Figure 5. At t = 1.42 sec the source voltage (v_s), load current (i_L) and load voltage (v_L) are balanced and sinusoidal under linear loads as observed from Figure 4 and Figure 5. A voltage swell of 20% is introduced under linear loads and non-linear load at t = 1.45 sec to 1.48 sec. The proposed ATILS Control Strategy based DVR introduces mitigating voltage in such manner that the load voltage (v_L) and load voltage (i_L) are sinusoidal and balanced, it was observed that from Figure 4 to Figure 5. The proposed ATILS control strategy based DVR in Figure 4 and Figure 5 from t = 1.42 sec to 1.48 sec the performance voltage (v_{dc}) and terminal voltage (v_t) of DVR are regulated to rated values at 200 V and 339 V as shown under linear/non-linear loads. During harmonic compensation of non-linear

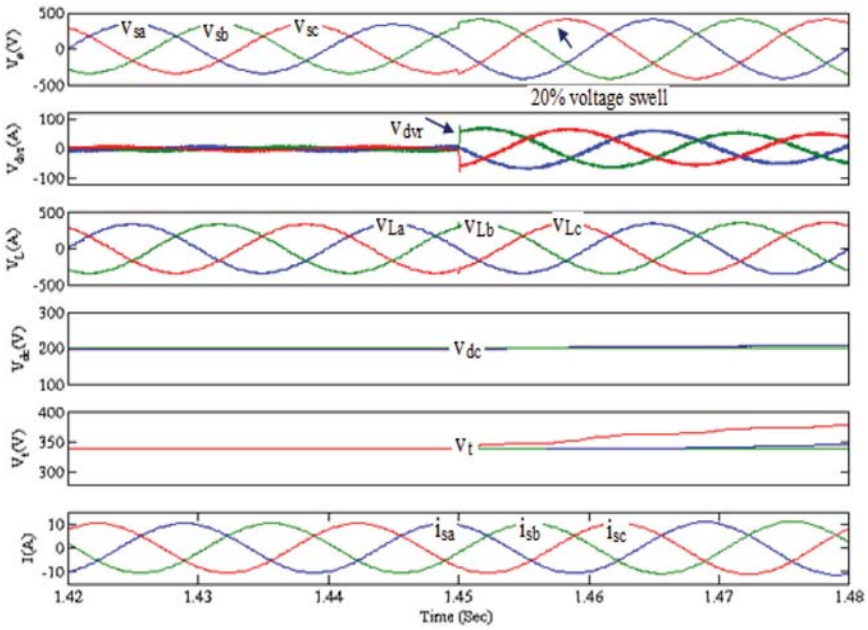

Figure 4 Performance of ATILS Control Strategy based DVR for 20% voltage swell under linear loads.

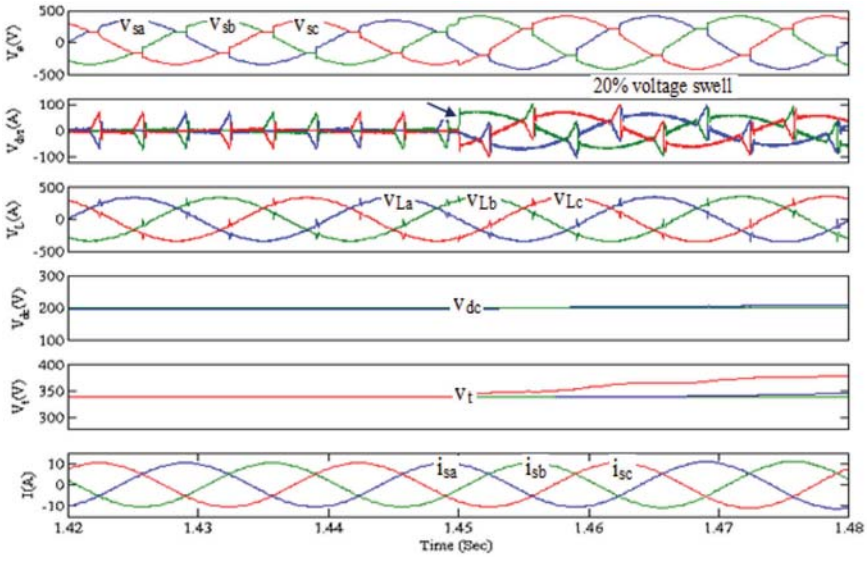

Figure 5 Performance of ATILS Control Strategy based DVR for 20% voltage swell under non-linear loads.

load condition, THD of source voltage (v_s) is 6.09% and THD of load voltage (v_L) is 2.35% which are shown in Figure 8. The proposed ATILS control strategy based DVR in Figure 4 to Figure 5 from t = 1.42 sec to 1.48 sec the performance parameters shows satisfactory results at voltage swell under linear/non-linear loads as per IEC and IEEE standards.

3.3 Performance of DVR based on ATILS Control Strategy in the Unbalanced Voltage Conditions

The dynamic performance of three-leg VSC based DVR on ATILS control strategy during voltage swell at linear/non-linear load is depicted in Figure 6 and Figure 7. The parameters of performance indices such as supply voltage (v_s), compensating voltage (v_{dvr}), load voltage (v_L), dc bus voltage bus voltage (v_{dc}), terminal voltage (v_t), load current (i_L) at (t = 1.42 sec to 1.48 sec) unbalanced linear loads are depicted in Figure 6–Figure 7. At t = 1.42 sec to 1.48 sec, when one of the phase voltage is reduced to 27% of the rated nominal voltage, it was observed from Figure 6 that load voltage (v_L) and load current (i_L) are balanced and sinusoidal. At t = 1.42 sec to 1.48 sec, when one of the phase voltage is increased to 16% of the rated voltage it was observed from

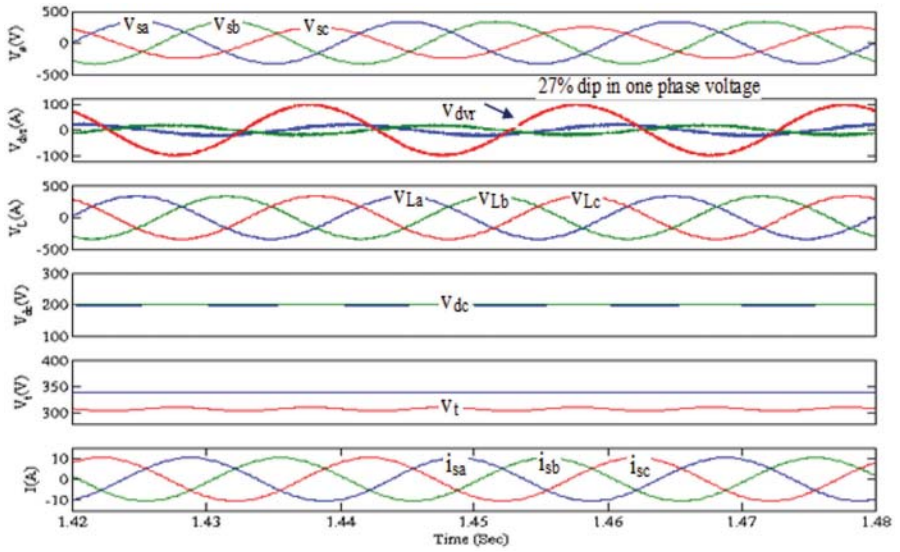

Figure 6 Performance of ATILS Control Strategy based DVR for unbalance load at 27% less voltage in one phase.

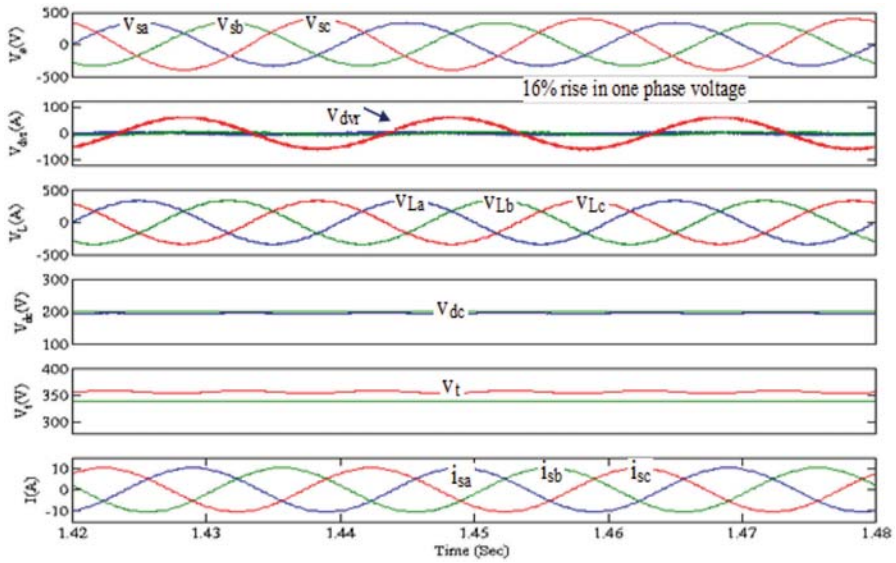

Figure 7 Performance of ATILS Control Strategy based DVR for unbalance load at 16% more voltage in one phase.

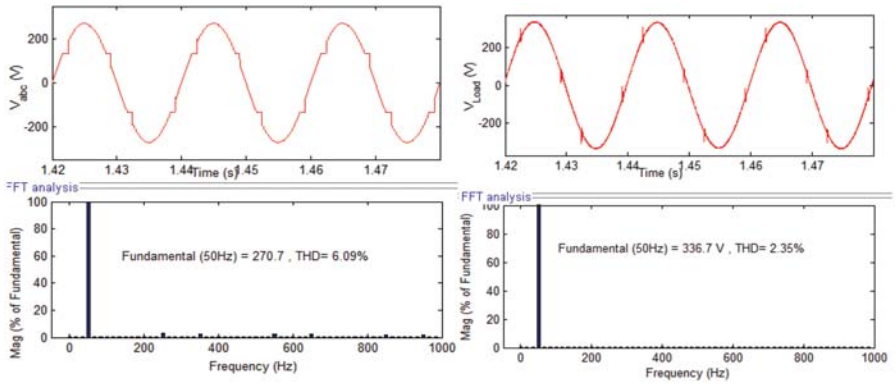

Figure 8 Source voltage and load voltage of harmonic spectra.

Figure 7 that load voltage (v_L) and load current (i_L) are balanced and pure sinusoidal. The Figure 6–Figure 7 shows that DVR injecting compensating voltage such that load voltage and load current are harmonic free under voltage and over voltage at the one phase. During unbalanced load conditions DVR maintains sensed dc bus voltage and terminal voltage at 200 V and 339 V.

The proposed ATILS control strategy based DVR in Figure 6 to Figure 7 from t = 1.42 sec to 1.48 sec the performance parameters shows satisfactory results at unbalanced voltage under linear/non-linear loads as per IEC and IEEE standards.

4 Real Time Hardware Implementation

A prototype 150 KVA, 415 V 50 Hz source and distribution load along with ATILS control strategy based DVR is developed and implemented using RT-LAB. A balanced linear R-L load is taken as linear load to demonstrate sag, swell, unbalanced voltages. A universal diode with R-L load is considered as consumer loads to demonstrate of harmonic Compensation. The ATILS control strategy based DVR is modeled and implemented using RT-LAB 8.2.5 with fixed step size of 35 μs and Runge-Kutta (ODE4 solver). A three leg VSC is used as DVR for a 150 KVA, 415 V 50 Hz Y-connected system at PCC through injecting transformer and inductor filter. A dc bus capacitor value of 3000 μF is used and is regulated at 200 V. Dynamic performance of ATILS control strategy based DVR are recorded using a Fluke 43B power analyzer.

5 Hardware Results and Discussion

The real time hardware results of ATILS control strategy based DVR under voltage sag/swell, harmonics compensation and unbalance voltages are shown in Figure 9–Figure 14. The parameters indices of distribution system such as supply voltage of 'a' phase (v_{sa}), compensating voltage (v_{dvr}), load voltage of 'a' phase (v_L), dc bus voltage (v_{dc}), source terminal voltage (v_{st}), load terminal voltage (v_{Lt}) are shown in Figure 9–Figure 14.

5.1 Hardware Results of ATILS Control Strategy based DVR under Voltage Sag

The hardware results of DVR on ATILS control strategy during voltage sag at linear load is depicted in Figure 9. A 20% of voltage sag is introduced under linear load condition. The proposed ATILS Control Strategy based DVR introduces mitigating voltage (v_{dvr}) in such a manner that load voltage (v_{La}) is balanced and sinusoidal and it maintains a voltage of 238.0 V. It was observed from Figure 9 that the dc bus voltage (v_{dc}) is maintained at 197.9 V. The source terminal voltage (v_{st}) and load terminal voltage (v_{Lt}) are maintained at 312.4 V and 347.3 V in the real time hardware.

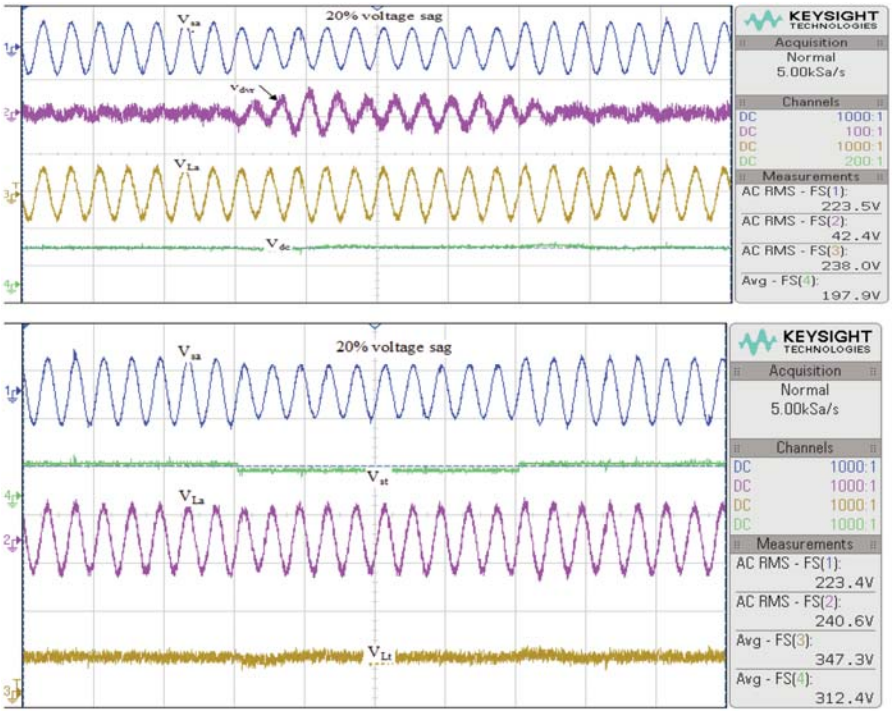

Figure 9 Hardware simulation of ATILS Control Strategy based DVR for 20% voltage sag.

5.2 Hardware Results of ATILS Control Strategy based DVR under Voltage Swell

The hardware results of DVR on ATILS control strategy during voltage swell at linear load is depicted in Figure 10. A voltage swell of 20% is introduced under linear load condition. The proposed ATILS Control Strategy based DVR introduces mitigating voltage (v_{dvr}) in such a manner that the load voltage (v_{La}) is balanced and sinusoidal and it maintains a voltage of 239.8 V. It was observed from Figure 10 that dc bus voltage (v_{dc}) is maintained at 194.0 V. The source terminal voltage (v_{st}) and load terminal voltage (v_{Lt}) are maintained at 368.8 V and 352.5 V in the real time hardware.

5.3 Hardware Results of ATILS Control Strategy based DVR under Harmonics Compensation

The hardware results of DVR on ATILS control strategy during harmonics compensation at non-linear load is depicted in Figure 11. A highly non-linear

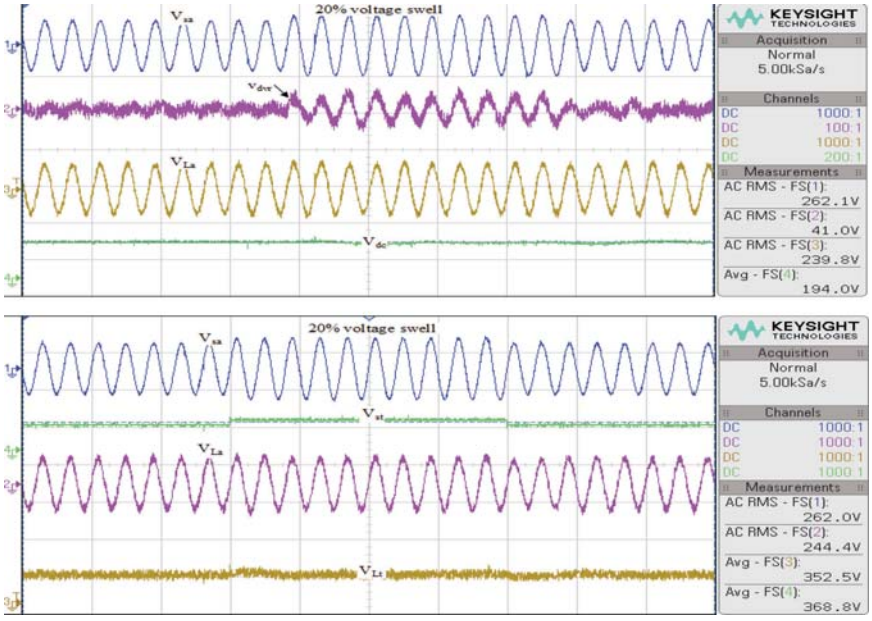

Figure 10 Hardware simulation of ATILS Control Strategy based DVR for 20% voltage swell.

load is connected at distribution load to demonstrate harmonics compensation. The proposed ATILS Control Strategy based DVR introduces mitigating voltage (v_{dvr}) in such a manner that load voltage (v_{La}) is purely sinusoidal, harmonic free and it maintains a voltage of 246 V. It was observed from Figure 11 that dc bus voltage (v_{dc}) is maintained at 191.8 V in the real time hardware. Fluke 43B power analyzer is used to demonstrate %THD of source voltage and load voltage. The source voltage of %THD of 8.9% and its fundamental voltage of 236.7 V whereas load voltage of %THD of 4.2% and its fundamental voltage of 240.0 V are shown in Figure 14.

5.4 Hardware Results of ATILS Control Strategy based DVR under Unbalanced Load

The hardware results of DVR on ATILS control strategy during unbalanced at linear load is depicted in Figure 12 and Figure 13. A 27% reduced voltage in 'c' phase is introduced compared to 'a' and 'b' phases under linear load condition. The proposed ATILS Control Strategy based DVR introduces mitigating voltage (v_{dvr}) in such a manner that load voltages (v_{La}, v_{Lb}, v_{Lc})

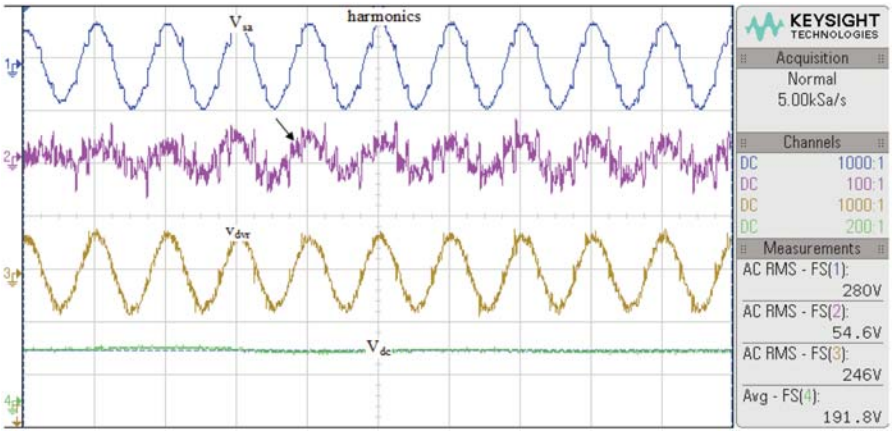

Figure 11 Hardware simulation of ATILS Control Strategy based DVR for harmonic compensation.

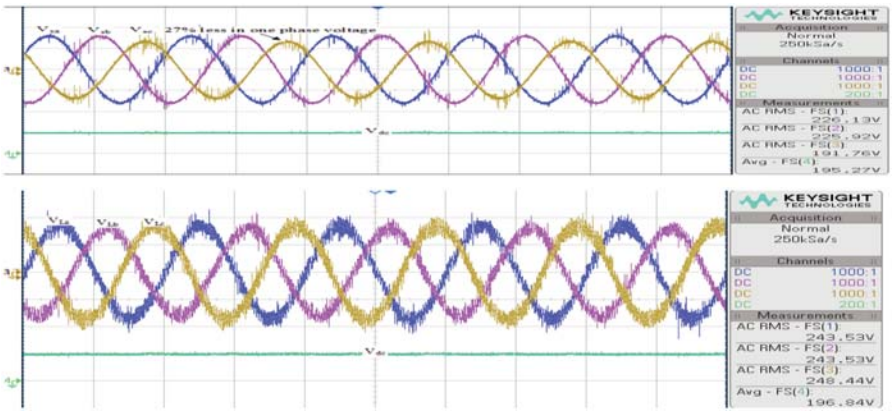

Figure 12 Hardware simulation of ATILS Control Strategy based DVR for unbalance load at 27% less voltage in one phase.

are purely sinusoidal and highly balanced. It was observed that from Figure 12 that dc bus voltage (v_{dc}) is maintained at 195.27 V in the real time hardware.

A 16% increased voltage in 'c' phase is introduced compared 'a' and 'b' phases under linear load condition. The proposed ATILS Control Strategy based DVR introduces mitigating voltage (v_{dvr}) in such a manner that load voltages (v_{La}, v_{Lb}, v_{Lc}) are purely sinusoidal, highly balanced. It was observed

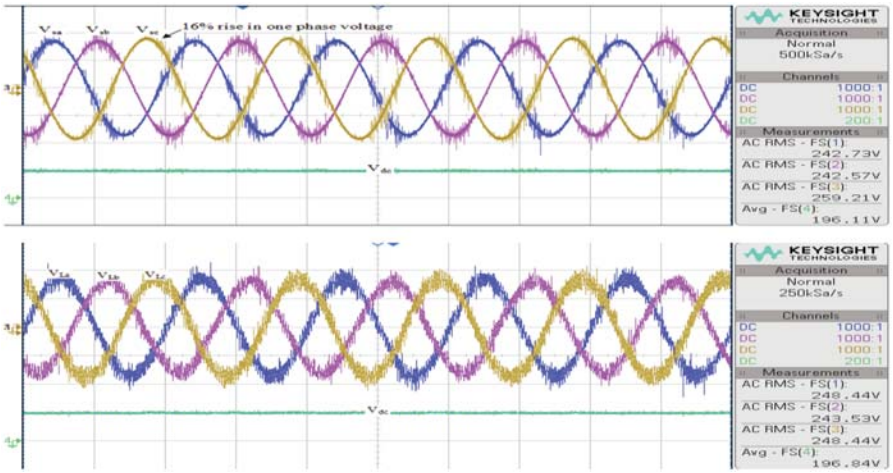

Figure 13 Hardware simulation of ATILS Control Strategy based DVR for unbalance load at 16% rise voltage in one phase.

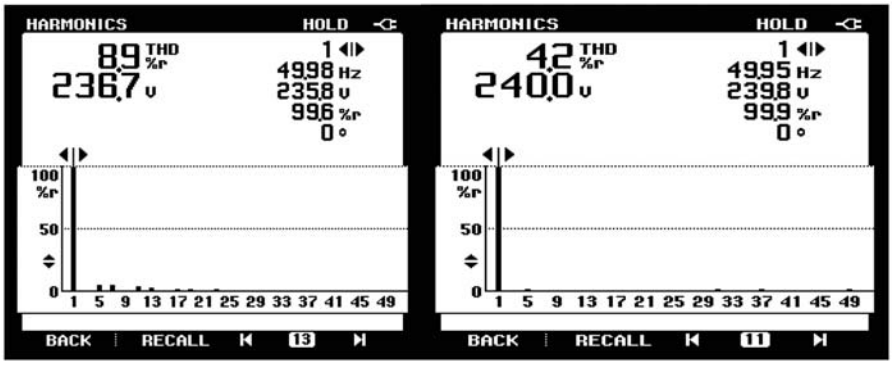

Figure 14 Real Time harmonic spectra of source voltage (v_s) and load voltage (vL).

that from Figure 14 that the dc bus voltage (v_{dc}) is maintained at 196.11 V in the real time hardware.

6 Conclusion

The three leg VSC based DVR is implemented by using ATILS Control Strategy. The proposed ATILS control strategy has been used for quick and accurate extraction of reference load voltages for generation of switching

pulses of DVR. The proposed DVR is more reliable, efficient and controls reactive power. The dynamic performance of ATILS Control Strategy based DVR shows satisfactory simulation results and hardware results for PQ problems such as compensation of voltage sag/swell under linear/non-linear loads and unbalanced voltage sag/swell. Under different PQ disturbances, the sensed dc bus voltage and terminal voltage are maintained at 200 V and 339 V respectively under MATLAB simulation and hardware results. In ATILS control strategy based DVR during harmonic compensation, THD of source voltage (v_s) is 6.09%, THD of load voltage (v_L) is 2.35% within IEC and IEEE standards under MATLAB simulation. In ATILS control strategy based DVR during harmonic compensation, THD of source voltage (v_s) is 8.9%, THD of load voltage (v_L) is 4.2% within IEC and IEEE standards under hardware.

Appendix

The ATILS Control Strategy based DVR parameters are:

Supply voltage: 415 V, 50 Hz
Source Impedance: $R_s = 0.1\ \Omega$, $L_s = 1$ mH
Consumer loads: Non-Linear Load – 3-Φ diode bridge rectifier with $R = 4\ \Omega$ and L = 500 mH.
Linear Load – 15 Ω and 100 mH
Ripple filter: $R_f = 5.0\ \Omega$ and $C_f = 5.0\ \mu$F (for 10 kHz PWM frequency)
DC voltage PI controller: $k_{p1} = 1.412$, $k_{i1} = 1.602$
AC voltage PI controller: $k_{p2} = 3.31$, $k_{q2} = 5.14$
DC bus capacitor $C_{dc} = 3000\ \mu$F
AC inductor: 2.99 mH
Transformer: 15 kVA, 100 V/400 V per transformer

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