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# A Differential Cascode Low Noise Amplifier Based on a Positive Feedback Gain Enhancement Technique

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Mingcan Cen and Shuxiang Song

*College of Electronic Engineering, Guangxi Normal University,  
Guilin, China*

*Corresponding Author: songshuxiang@mailbox.gxnu.edu.cn*

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## Abstract

This paper presents a differential low noise amplifier (LNA) based on a new configuration suitable for low-power and low noise applications. By inserting additional positive feedback capacitor connected to drain and source terminal of the cascode transistor, this proposed configuration increases voltage gain because of decreasing the total transconductance by a factor generated a negative conductance. In addition, the differential structure and power-constrained simultaneous noise and input matching (PCSNIM) technique are chosen simultaneously to perform the input matching and to improve the noise figure at the desired band. Using TSMC 0.18  $\mu\text{m}$  RF CMOS process, the proposed LNA exhibit a state of the art performance consuming only 7.58 mW from a 1.8 V power supply. Input and output return loss of the LNA are below than  $-13\text{dB}$  while achieves a power gain of 18.66 dB and a noise figure of 2.03 dB at the band of interest.

**Keywords:** low noise amplifier, gain, positive feedback, transconductance.

## 1 Introduction

With the accelerated development of high performance wireless communication systems like cellular systems, global navigation satellite system (GNSS), wireless local area network (WLAN), Blue-tooth, Mobile TV and etc, the demand for high performance, high integrated and low cost radio frequency (RF) receiver for portable wireless communication systems has considerably grown in consumer electronics market. In millimetre-wave receiver design, the low-noise amplifier (LNA) is a critical building block that amplifies the received signal and contributes most of the noise figure of the whole receiver [1]. The LNA design involves trade-offs between noise-figure (NF), gain, power dissipation, input matching, and harmonic content in the output signal [2]. In addition, with the rapid development of integrated circuit technology, the high integrated and small chip circuit shows the advantage for battery-powered portable applications. But with the decrease of chip size, it has become a challenge to improve the performance of the LNA circuit, such as power gain and noise figure in a limitation area.

To achieve higher gain and lower noise performance, many kinds of narrow band LNA topologies [2–4] have been proposed as a way to satisfy this requirement for low power dissipation. In these topologies, typically by improving the structure to increase the linearity, reduce the noise figure or the chip size. Traditional methods usually try to improve the gain of the amplifier by increasing the effective transconductance of the circuit. In contrast to conventional methods, we proposed in this work a positive feedback gain-enhanced technique based on the positive feedback capacitor, as a way to improve the gain of the amplifier. It is shown, by means of feedback capacitor, that the proposed technique decreases the output total transconductance at the drain of the output transistor by generating a negative conductance. Moreover, by this gain-enhanced technique, the gain of the LNA has been increased effectively from 15.76 dB to 18.66 dB without sacrificing bandwidth, linearity, noise and current consumption.

This paper is organized as follows. In Section 2, the description including the PCSNIM technique, the proposed positive feedback gain enhancement technique, the analysis of the stability and the proposed LNA circuit. Section 3 presents the simulation results, discussed and finally compared to those of the recent works. Section 5 concludes the achievements and results.

## 2 Circuit Design and Analysis

### 2.1 LNA Topology with the PCSNIM

Figure 1 shows the typical amplifier circuit using the power-constrained simultaneous noise and input matching (PCSNIM) technique. This well-known technique is usually used to achieve simultaneous input impedance and minimum noise matching, as mentioned in [5]. If the gate resistance and the total parasitic capacitances except the gate-to-source capacitances are neglected, the overall input impedance of this LNA can be expressed as

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega(c_{gs1} + c_{ex})} + \frac{g_{m1}}{c_{gs1} + c_{ex}}L_s \quad (1)$$

Where  $C_{ex}$ ,  $C_{gs1}$  and  $g_{m1}$  are the additional capacitor, the intrinsic gate-to-source capacitor and the transconductance of M1, respectively. Their values are chosen according to PCSNIM technique with corner frequency of 5.8 GHz selected in order to achieve a good input reflection coefficient.

The Circuit of equivalent transconductance calculation is shown in Figure 2, to evaluate equivalent transconductance  $G_m$ , the following equation can be given

$$i_y = g_{m1}v_{gs1} \quad (2)$$

$$v_{in} = j\omega(C_{gs1} + C_{ex})v_{gs1} \times (R_s + j\omega L_g) + v_{gs1} + j\omega L_s [g_{m1}v_{gs1} + j\omega(C_{gs1} + C_{ex})v_{gs1}] \quad (3)$$

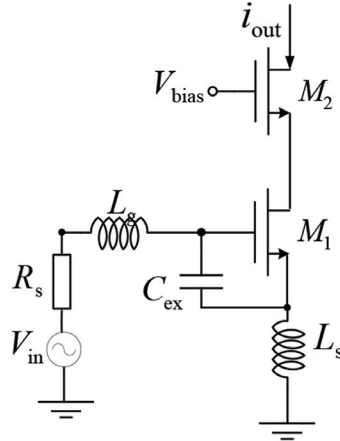
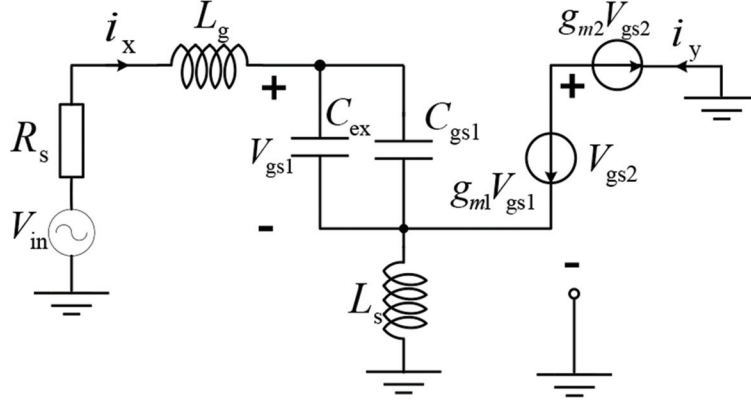


Figure 1 Conventional cascode LNA.

Figure 2  $G_m$  calculation.

then

$$G_m(j\omega) = \frac{i_y}{v_{in}}(s) = \frac{g_{m1}}{1 + j\omega[g_{m1}L_s + R_s(C_{gs1} + C_{ex})] - \omega^2(C_{gs1} + C_{ex})(L_s + L_g)} \quad (4)$$

The equivalent transconductance  $G_{m,eff}$  at resonant frequency is then got by

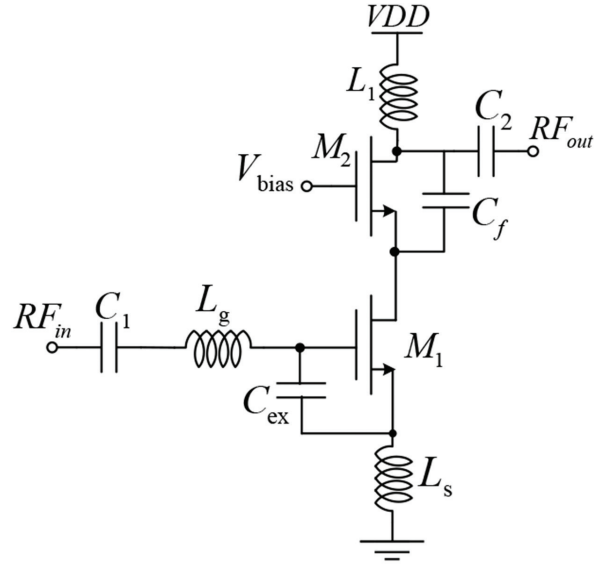
$$G_{m,eff} = |G_m(j\omega_0)| = g_{m1}Q_{in} = \frac{g_{m1}}{2\omega_0(C_{gs1} + C_{ex})R_s} \quad (5)$$

Where  $Q_{in} = 1/[2R_s\omega_0(C_{gs1} + C_{ex})]$  is the quality factor of the series resonating input matching circuit.

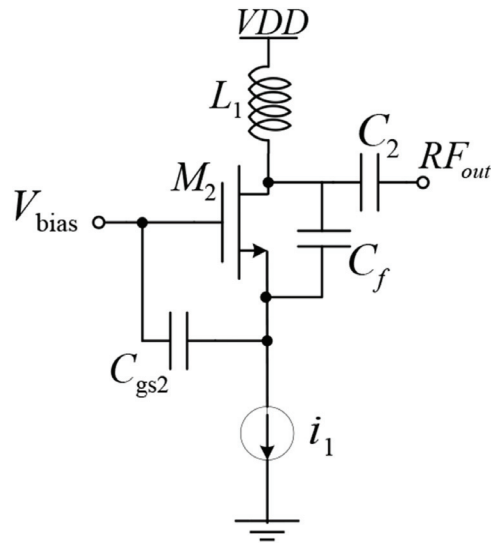
## 2.2 The Proposed Topology

The LNA with the proposed positive feedback gain-enhanced technique is demonstrated in Figure 3. In this topology, a positive feedback capacitance  $C_f$  is inserted between the source and drain terminal of the transistor M2. This phenomenon can be understood by another point of view as the form of oscillator. The capacitors  $C_{gs2}$ ,  $C_f$  and transistor M2 constitute an oscillator topology with inductive termination at the output. Referring again to Figure 1, the gain of the LNA circuit without the feedback  $C_f$  can be expressed as [3]

$$A_v = g_{m1}Q_{in}R_{load} = g_{m1}Q_{in}(1/G_{tot}) = G_{m,eff}(1/G_{tot}) \quad (6)$$



(a)



(b)

**Figure 3** (a) LNA with the proposed gain enhancement architecture, (b) simplified equivalent circuit of Figure 3 (a).

Where  $G_{tot}$  is the total transconductance at the drain of M2 and is dominated by the equivalent parallel conductance of the inductor ( $G_p$ )

$$G_P = 1/Q_{L1}^2 R_{L1} \quad (7)$$

Where  $R_{L1}$  and  $Q_{L1}$  are the series resistance and quality factor of inductance  $L_1$ , respectively. In addition, the LNA gain is proportional to the inductor quality factor and the inductor value as shown below [3]

$$Gain \propto R_P \propto Q_{L1}^2 R_{L1} \propto \omega_0 Q_{L1} L_1 \quad (8)$$

Where  $R_P$  is the parallel resistance of  $L_1$  obtained from the series to parallel transformation. The above analysis shows that the gain of the circuit can be increased by larger  $G_{m,eff}$  or larger  $L_1$ .

Assume that  $\omega_0 \ll g_{m2}/(C_{gs2} + C_f)$ , from the Figure 3 (b), the negative conductance is generated by  $C_f$  is

$$G_N = \omega_0^2 C_{gs2} (C_N + C_{gd2}) / g_{m2} \quad (9)$$

So the total transconductance now can be expressed as

$$G_{tot}^{\wedge} = G_P - G_N \quad (10)$$

The gain of the LNA with a feedback capacitance becomes

$$A'_v = g_{m1} Q_{in} (1/G_{tot}^{\wedge}) = G_{m,eff} (1/G_{tot}^{\wedge}) \quad (11)$$

The  $A'_v$  of the cascode LNA with the proposed technique has the same expression as (6) but with different  $G_{tot}$  as defined by (10). It is observed that the total transconductance from the drain of M2 decrease by times with the increasing feedback, while those from  $C_f$  increase. Since no active device is used, this does not increase the power consumption and additional noise. Therefore, the proposed topology provides much higher voltage gain with a help of increased output impedance. The simulation results in Figure 4 and Figure 5 have further confirmed that the voltage gain of the amplifier increases with the increase of capacitor. However, the variation of capacitance will slightly change the matching bandwidth. More important is that large capacitance can deepen feedback degree, for what will degenerate the gain and the stability of the LNA. Furthermore, the choice of  $C_f$  must consider the efficiency of stability of the LNA as well as the moderate gain.

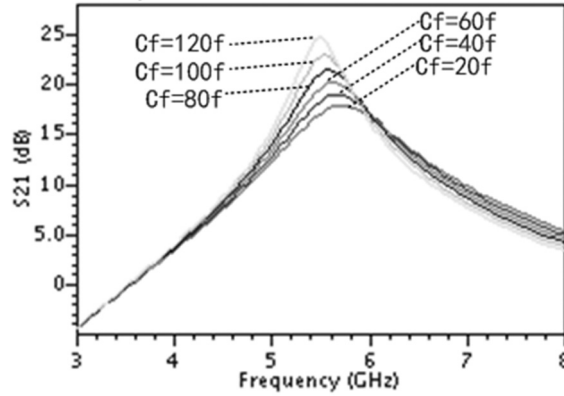


Figure 4 Simulated the gain  $S_{21}$  versus frequency with different values of  $C_f$ .

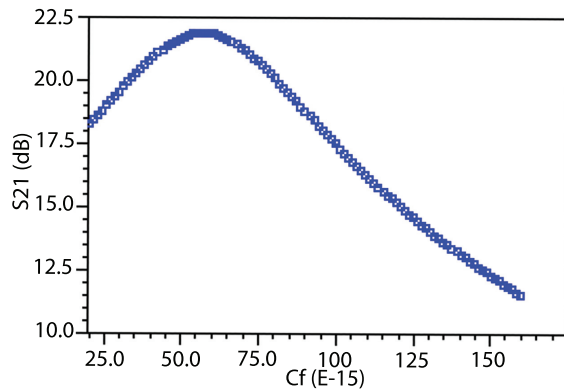


Figure 5 Simulated the gain  $S_{21}$  at 5.8 GHz with different values of  $C_f$ .

### 2.3 Analysis Stability

The stability of the LNA is defined as [3]

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad (12)$$

where  $|\Delta| = S_{11}S_{22} - S_{12}S_{21}$ .

The unconditional stability requirement of LNA is  $K > 1$  and  $|\Delta| < 1$  [3]. Compared with the typical LNA topology, the added positive feedback capacitor  $C_f$  forms a signal path from the drain of the transistor M2 to the source of M2, which will also increase the instability of the LNA. The limit to amount of feedback is governed by stability consideration. To ensure the unconditional

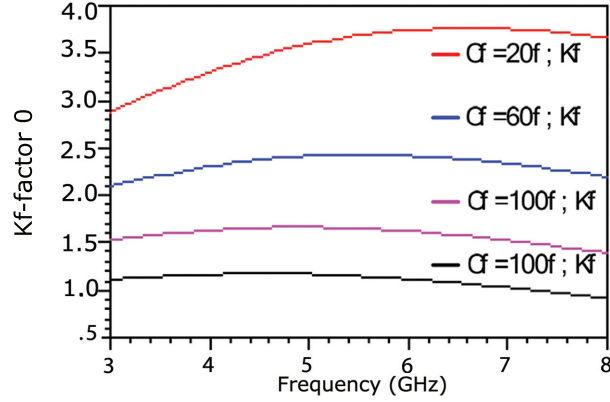


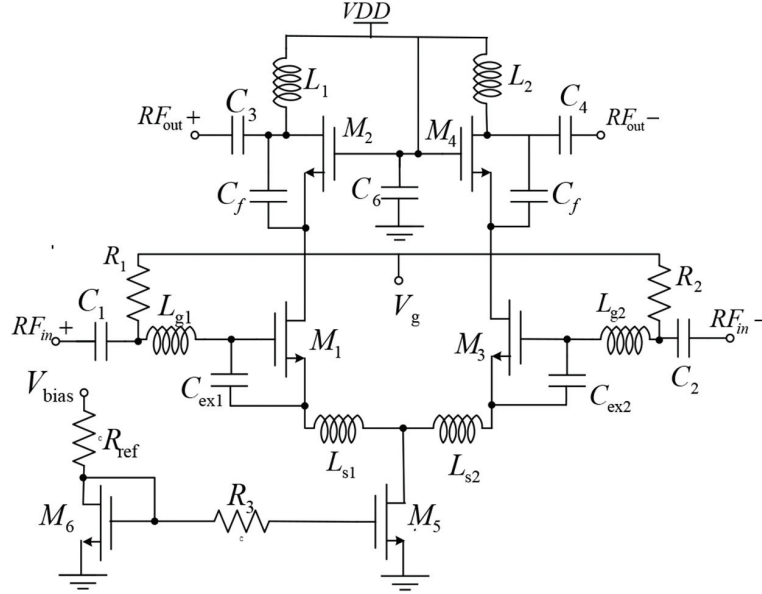
Figure 6  $C_f$  effect on LNA stability factor  $K_f$ .

stability,  $G_{tot}$  must be always positive. To further confirm the effect of feedback capacitor and to perform a comparison, the case with different value of feedback capacitor is simulated with the same power dissipation, as shown in Figure 6. From this we can see that large capacitance will weaken the stability of the circuit, so the capacitor selection should take into account the stability.

## 2.4 Proposed LNA Circuit Topology

The proposed gain enhancement LNA topology with positive feedback capacitor is depicted in Figure 7. The differential topology presents a better rejection to common mode interferences unity to some packaging components, a better linearity and gain although it does have its inconveniences, such as a larger consumption and it occupies a larger area. Due to its advantages, we still use this topology. The positive-feedback loop is implemented by adding couple capacitors between the drain and source of the output transistors (M2, M4) and their value should be chosen tradeoff with the gain and stability. The feedback capacitors can increase the chip size, but we will not consider this, because that the gain can be increased at a much higher rate than size. The differential input signals through the transistors M1, M3 will be injected to the source of the transistors, M2 and M4, and these are coupled to the sources of the transistors through capacitors to form feedback path. By this way, the gain will be improved as analysis in Section 2.2.

In Figure 7, the input matching network is consisted by  $C_{ex}$  and  $L_s$  and their size are chosen following the design principle of the PCSNIM



**Figure 7** The schematic of the gain-enhanced differential LNA with positive feedback.

technique [5]. The inductors ( $L_{g1}$ ,  $L_{g2}$ ) are inserted for the input matching to the signal source impedance of  $50 \Omega$  at the operating frequency (5.8 GHz) and therefore their size depends on the input transistor size. When selecting the input transistor's size, a major design tradeoff is that the current density required for minimum noise figure [12]. In order to obtain the best noise performance, the optimum width of the input transistors ( $M_1$ ,  $M_3$ ) was chosen here according to [12], where the noise figure was optimized under power constrain.

$$W_{opt} \cong \frac{1}{3\omega LC_{ox}R_s} \quad (13)$$

Where  $\omega$ ,  $L$ ,  $C_{ox}$  and  $R_s$  are the operating frequency, the length of the input transistors, the gate capacitance per area and the source resistance, respectively. According to [5], once those devices size are determined, the optimum impedance needed to be matched to the optimal noise matching is also determined. The transistors  $M_5$ ,  $M_7$  and resistances  $R_1$ ,  $R_3$  are served as a current mirror with a reference current as bias circuit. The chosen biasing topology establishes a reference current determined by the value of  $R_{ref}$ , while  $R_3$  is chosen to be big enough so that the loading effect of the bias circuit on the signal path is negligible. In this circuit, the length

of all the transistors are adopted the minimum channel length 0.18  $\mu\text{m}$  to obtain a higher cutoff frequency. The sizes of the devices on the symmetrical structure have the same parameters. The main component parameters of the LNA are listed as follows: the biased voltage of M1 and M2 are 1.5 V, the gate-width of M1 and M2 are 102.6  $\mu\text{m}$ . Considering the LNA should work at unconditionally stable working condition, the value of feedback capacitance  $C_f$  choose 0.025  $pF$ .

### 3 Simulation Results and Discussions

The differential LNA has been designed in TSMC 0.18  $\mu\text{m}$  CMOS RF process. Simulations have been performed using Cadence Spectre RF. Using a supply voltage of 1.8 V, the designed LNA including the bias circuit draw only 4.21 mA resulting in a power consumption of 7.58 mW. This is relatively low for a 5.8 GHz CMOS differential LNA with a power gain greater than 18.66 dB. Figure 8 shows the simulated scattering parameters of the LNA. In the operating frequency of 5.8 GHz, a power gain  $S_{21}$  of 18.66 dB is achieved. The input return and output return losses ( $S_{11}$ ,  $S_{22}$ ) of the LNA are  $-13.73$  dB and  $-14.68$  dB at 5.8 GHz, respectively. The Reverse isolation is  $-23.01$  dB; that good reverse isolation is due to utilizing cascode structure.

To show the effects of the positive feedback capacitor on the frequency response of the gain, the schematic simulation results are illustrated in Figure 9. The obtained results clearly illustrate the important role of the capacitor in improving the gain performance in high frequency. This improvement is obtained by decreasing the total transconductance at the drain of the output transistor by a factor that generated a negative conductance.

Figure 10 shows that the proposed LNA achieves a noise figure 2.04 dB at the central frequency 5.8 GHz, and with a NF ripple of  $\pm 0.01$  dB in the frequency range of 5.725–5.825 GHz, which is excellent compared to recently reported designs. Note that, the NF of the LNA coincides with  $NF_{\min} = 1.86$  dB very well at the frequency of 5.8 GHz. Figure 11 shows the simulation result of the input 1-dB compression point (IP1dB). An input sinusoidal signal with a frequency of 5.8 GHz is used. The value of IP1dB is about  $-17.26$  dBm.

Table 1 summarizes the performance of the proposed CMOS differential LNA compared to the recently reported literatures. As can be seen from Table 1, the proposed differential LNA achieves a lower noise figure, a higher

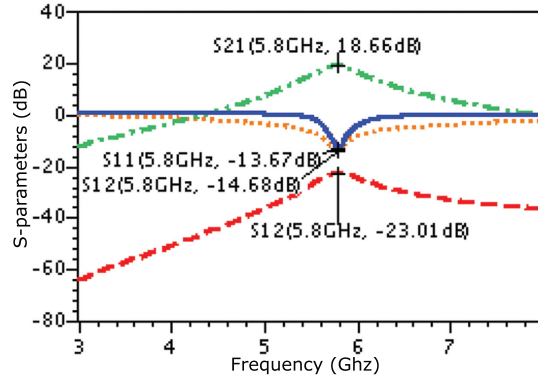


Figure 8 Simulated S-parameters of the LNA.

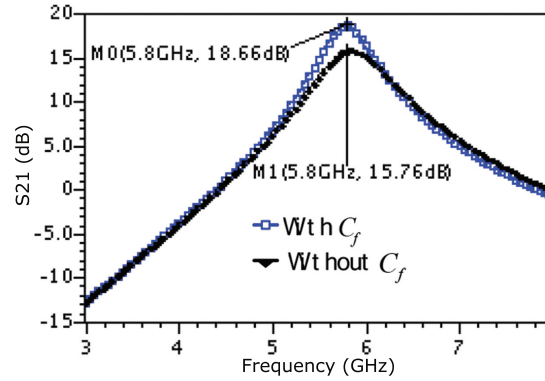


Figure 9 Voltage gain simulation results of the LNA with and without  $C_f$ .

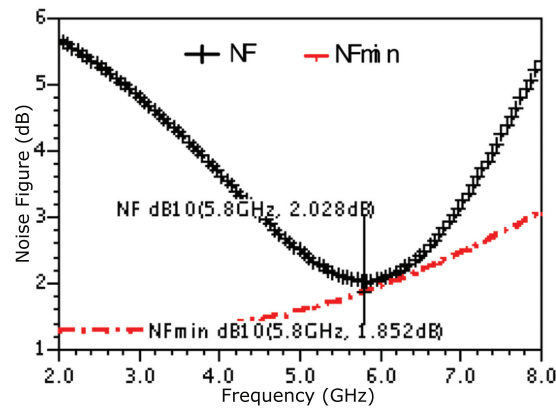
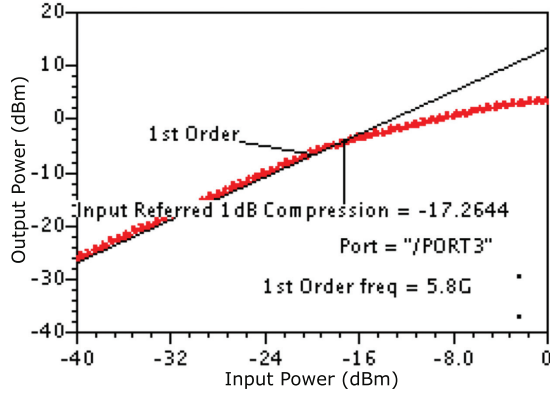


Figure 10 The simulation of noise figure.



**Figure 11** The simulation result of the input 1-dB compression point.

voltage gain, and a smaller power dissipation compared to prior techniques listed. These results demonstrate that the proposed technique has an advantage in improving the gain of the LNA circuit, while considering differential topology.

**Table 1** Comparison between this work and other reported literatures

Ref.	Technology	Topology	Freq (GHz)	NF (dB)	Pdc (mW)	S21 (dB)
[2]	0.18 um (SOI)	Single-ended	5.0	0.95	12.0	12.0
[6]	0.18 um (CMOS)	Fully-differential	5.7	3.65	14.4	14.5
[7]	0.13 um (CMOS)	Fully-differential	5.0	2.62	10.3	18.0
[8]	0.18 um (CMOS)	IPD-differential	5.2	2.1	10.0	15.5
[9]	0.13 um (CMOS)	Fully-differential	5.2	2.9	8.0	21.0
[10]	0.13 um (CMOS)	differential	5.0	2.16	10.3	16.2
[11]	0.09 μm (CMOS)	differential	5.8	1.7	19.6	12.0
This work	0.18 um (CMOS)	differential	5.8	2.03	7.58	18.66

## 4 Conclusion

In this paper, a gain enhancement technique using positive feedback for a cascode differential LNA was proposed. Simulation result has shown that, depending on the conventional cascode structure and the proposed design methodology, the gain of the LNA can be significantly improved due to an additional positive feedback capacitor, which decreases the total transconductance at the drain of the output transistor by a factor that generated a negative conductance. Using a  $0.18\ \mu\text{m}$  CMOS process, the presented LNA topology consumes only 7.58 mW from a 1.8 V supply voltage and achieves a power gain of 18.66 dB at the operating frequency 5.8 GHz. Considering the performance achieved, the proposed techniques is suitable for the implementation of narrowband LNAs in wireless receivers.

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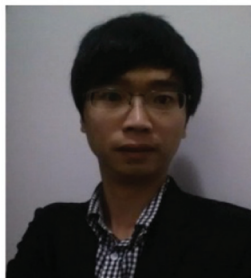
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## **Biographies**



**M. Cen** received the B.S. degree in microelectronics from the Guilin University of Electronic Technology, in 2007, Guilin of China. He is currently a teaching assistant at Department of College of Electronic Engineering, Guangxi Normal University, Guilin of China. His research interests include CMOS RF/analog IC design for wireless application.



**S. Song** received the B.S degree in compute engineering at National University of Defense, Changsha of China and the M.S. degree in microelectronics Guilin Institute of Electronic Technology, Guilin of China and Ph.D. degrees in microelectronics at Huazhong University of Science and Technology, Wuhan of China. He is now a Professor with the College of Electronic Engineering, Guangxi Normal University and a master director of integrated circuit design, VLSI, and Microelectronics at Guangxi Normal University. His research interests include high speed CMOS A/D converters, VLSI technology, LNA design, Analog Integrated Filter Circuits.

