Smart Power Analysis for Digital Circuits using Machine Learning

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5.4. *Abstract.*

One of the most critical factors in modern design and optimization is power consumption in digital circuits, especially for energy-efficient systems. In this project, it has been shown how power consumption in logic circuits can be estimated by implementing machine learning types based on its structural characteristics. The input features in this instance would be parameters like the amount of gates, logic components AND, OR, NAND, NOR, inverters, flip flops, inputs, outputs, and so on. Having these various feature values, several regression patterns are learned and their actions are calculated for distinct measures like MAE, MSE, RMSE, R^2, MAPE using Linear Regression, Ridge, Lasso, ElasticNet, Decision Tree, Random Forest regressors. The outcome of research is a valid power consumption estimation method that will be helpful for circuit designers in optimizing the components to get better energy efficiency.

Keywords. Power Consumption Prediction, Machine Learning, ISCAS-89 Benchmark, Regression Models, Random Forest.

1. *INTRODUCTION*

Power estimation is the important aspects of digital VLSI circuit design and plays a crucial role in energy consumption, general efficiency, and sustainability regarding electronic devices. Regarding this aspect, accurate power advance estimation is mainly needed for design optimization, and observance of thermal and energy constraints. Conventionally, power dissipation has been performed through analytical modeling and simulations at various levels of abstraction, such as system-level, RTL- level, gate-level, and transistor-

level analysis. While higher-level abstractions present results faster but with lower accuracy, the low-level analysis gives very accurate estimates; however, it is computationally expensive and time-consuming. Recent advances in machine learning have brought a paradigm shift in power estimation. In the context of logic-level abstractions, this is related to a number of critical factors, such as the quantity of logic elements, gates, input/output ports, and flip-flops. This paper proposes a novel methodology for power prediction in sequential digital circuits utilizing machine learning algorithms. The circuit involved feature extraction from the ISCAS-89 benchmark dataset, which included gate count, flip-flops, and logic gates. Regressions including simple Regression models, Decision Tree, and Random Forest, are instructed to predict power consumption.

2. DATA AND METHODOLOGY

A. Dataset

The input data employed in this paper is dependent on the ISCAS-89 benchmark circuits. This dataset contains a collection of multiple types of digital circuits, for all of which a single feature was extracted resulting from overriding design parameters associated with power consumption. It includes the following GATE Amount of logic gates AND, OR, NOR, NAND, INV. The count of the respective logic components within the circuit. This is followed by DFF Amount of flip-flops, which are sequential elements. Thirdly, IN and OUT represent Number of input and output ports correspondingly.

B. Methodology

The methodology involves the following steps:

1) Data Preprocessing:

Each and every characteristics are increased by Standard Scaler to regularize their ranges. Features and target variable were examined to identify power consumption.

2) Model Selection:

Six typical machine learning models were selected:

Simple Regression models, Decision Tree Regression and Random Forest Regression.

3) Training and Validation:

These regression models are instructed by utilizing the train dataset. A cross-validation strategy ensured robust evaluation and reduced overfitting risks.

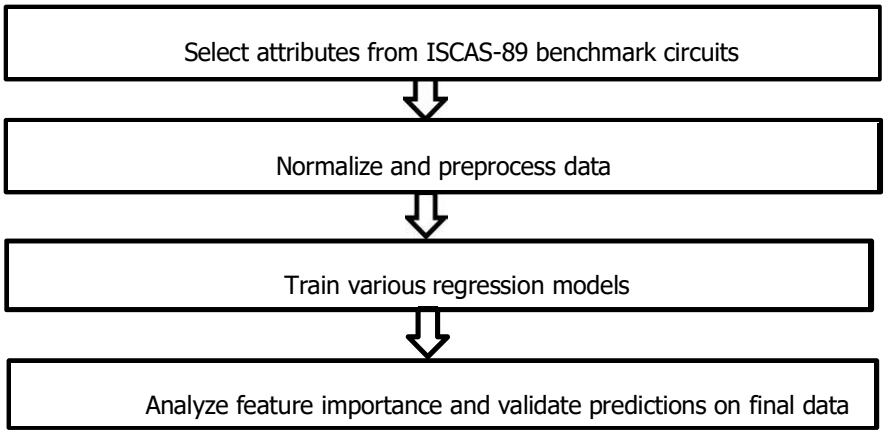
4) Feature Importance Analysis:

Feature importance ranking was performed using the Random Forest model, highlighting parameters like the number of gates and flip-flops.

5) Model Evaluation:

Regression models are compared based on error metrics and R^2 values.

C. Flow Of Methodology



D. Metrics

The simply absolute deviation is the mean of the complete difference between the real and the estimated values in the dataset. 1

$$MAE = \frac{1}{N}\sum_{i=0} |n - n1|$$

Where n1 - estimated value of n

n - mean value of n

Mean Squared Error: it calculates the average squared deviation of estimated values from the real values.

$$MSE = \frac{1}{N}\sum_{i=0}^{N} (n - n1)^2$$

Root Mean Square Error: square root of Mean Squared error. Indicating prediction dispersion.

$$MSE = \sqrt{MSE} = \sqrt{\frac{1}{N}\sum_{i=0}^{N} (n - n1)^2}$$

R-squared: Indicates how much of the variance in the dependent variable is explained by the model.

$$R^2 = 1 - \frac{\sum(n_i - n1)^2}{\sum(n_i - n)^2}$$

Adjusted R squared is a modification of R square. It takes into consideration the figure of manipulated variables in the model as well as it is always less than or equal to R^2.

$$R_{adj}^2 = 1 - \left[\frac{(1 - R^2)(m - 1)}{m - k - 1}\right]$$

3. RESULTS AND DISCUSSION

	MAE	MSE	RMSE	R^2	MAPE
Linear Regression	0.009551	0.000149	0.012195	0.999412	30.149286
Ridge Regression	0.014301	0.000415	0.020379	0.998358	27.918547
Lasso Regression	0.360856	0.252846	0.502837	0.000000	1079.966974
ElasticNet Regression	0.360856	0.252846	0.502837	0.000000	1079.966974
Decision Tree Regression	0.000000	0.000000	0.000000	1.000000	0.000000
Random Forest Regression	0.034864	0.005949	0.077127	0.976473	34.635113

Table 1: Model Performance

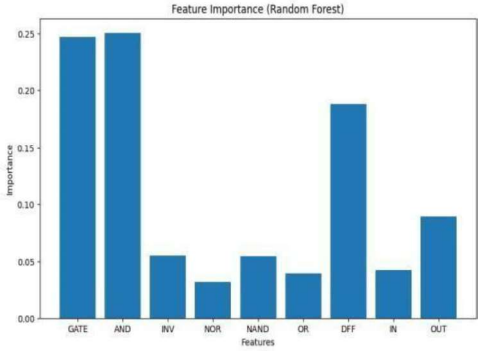


fig 1: Feature Importance for Power Estimation

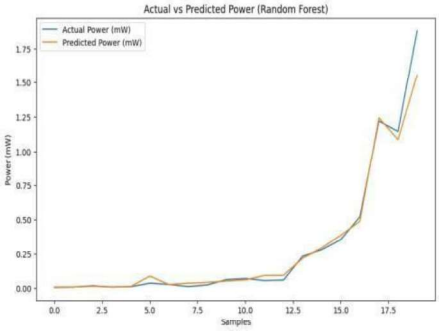


fig 2: Predicted vs Actual Power

6. 4 REFERENCES

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Ms. Sheik Shabeena is an Assistant Professor in the Department of Electronics and Communication Engineering (ECE) at Dadi Institute of Engineering & Technology Autonomous, Visakhapatnam. She completed her B.Tech in ECE from Avanthi Institute of Engineering & Technology in 2013 and her M.Tech in VLSI Design from MVGR College of Engineering in 2016. Currently, she is pursuing her Ph.D. at GITAM University, specializing in flip-flops and their applications in digital circuits. She has shown a deep passion for research and has authored 10 research papers on various topics within the realm of VLSI, digital systems, low-power design, embedded systems, and FPGA-based design.

Gavara Likhitha is a final-year Bachelor's student in Electronics and Communication Engineering at Dadi Institute of Engineering and Technology. She is an ambitious and diligent learner, striving for excellence.

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