Configurable Phase Locked Loop using Multi-Oscillator Feedback

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Abstract

This paper proposes and presents the design of a configurable Phase Locked Loop (PLL) working at wide band of frequency ranges from 150 MHz to 1.3 GHz achieved by frequency divider circuit and configurable Voltage Control Oscillator (VCO) proposed here. The design of differential delay cell is carried out which is used in the even staged Voltage Controlled Oscillator (VCO). The configurable component proposed is a sub-VCO which is connected along with the multiplexer to the 4 stage main VCO. This makes the VCO section as fourteen stage VCO with the sub-VCO block giving flexibility of choosing different PLL frequencies. The frequency divider circuit is given as feedback and is designed using True Signal-Phase Clock (TSPC) based D flip flop so that it can be used for both lower and higher frequency division. This PLL operates at four different conditions as per two enable input combinations (2^2). The proposed architecture of the PLL is implemented using 45nm technology node in Cadence IDE.

Keywords. Configurable PLL, VCO, sub-VCO, TSPC, frequency divider, enable signals, phase detector, charge Pump.

1. INTRODUCTION

A Configurable Phase-Locked Loop is an adaptable customize the PLL for various applications without the need for circuit redesign electronic circuit that can be dynamically adjusted or programmed to meet specific requirements. In contrast to traditional PLLs, [11], [12] which have fixed characteristics like frequency range and loop parameters, configurable PLLs offer flexibility in their operating parameters. This adaptability enables designers to customize the PLL for various applications without the need for circuit redesign.

The design of 4 stage and 14 stage convertible CMOS differential ring voltage controlled oscillator [3] is designed in 45nm technology, the differential delay cell [1] is designed and used in the oscillator. The Gain of the VCO is kept as low as possible to reduce the Phase noise and Jitter [4]. The 4-stage VCO oscillates at the frequency range of 1.35 GHz to 1.44 GHz and the 14-stage VCO oscillates at the frequency range of 295MHz to 326MHz.

The phase detector is designed for the PLL as in [5], positive edge triggered DFF is used along with the reset. The charge pump [6] is used along with loop filter in the PLL, which receives the up and down signals from the PFD and produces an error voltage. A True Single-Phase Clock (TSPC) flip flop [7] is used for frequency division, where the frequency is divided by 2.

2. ARCHITECTURE

2.1 VOLTAGE CONTROL OSCILLATOR

In the proposed design, VCO is designed using basic blocks called delay cells, differential delay cell [3] is used in the proposed VCO. The circuit of the mentioned delay cell is given as per Fig.1.

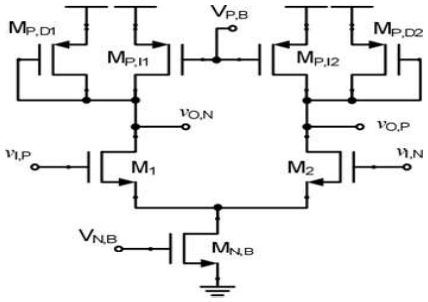

Figure 1 Circuit of differential Delay Cell

This is the differential delay cell [3] used in the design. The delay cell is sized to maintain a low differential gain, minimizing phase noise and jitter [10]. In this design, MN, B serves as the current source transistor for biasing the NMOS differential pair (M1/M2). The load of the delay cell includes diode-connected transistors (MP, D1/2) and a current source (MP, I1/2).

The series combination of this delay cell is used to design the ring VCO. The number of stages of delay cells decides frequency of operation of the VCO. A configurable VCO is designed by inserting an enable signal En1 along with multiplexer in between VCO and sub-VCO. The design of configurable VCO is shown in Fig.2. The configurable VCO includes a main VCO with 4 stages of delay cells in a cross- coupled arrangement and a sub-VCO with 10 stages of delay cells. Depending on the application and the required frequency, the number of delay cell stages in the sub-VCO can be adjusted.

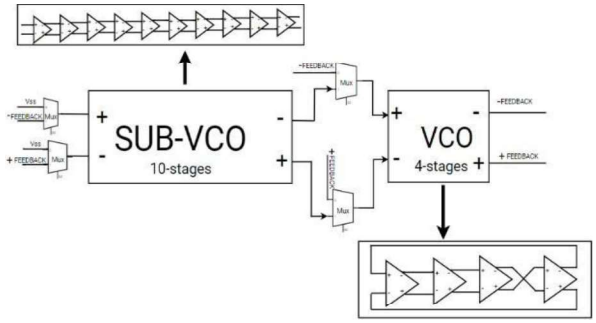

Figure 2 Proposed schematic of configurable VCO

2.2 Configurable Phase Locked Loop (PLL)

A PLL operates within a frequency range determined by the VCO's frequency range. Adjusting this frequency range typically requires modifications to the VCO's delay cell design. This paper introduces an architecture for a VCO where the frequency range can be adjusted using enable signals. The number of stages in the sub-VCO is varied based on the required frequency range. The modified architecture from [9] is illustrated in Fig. 6.

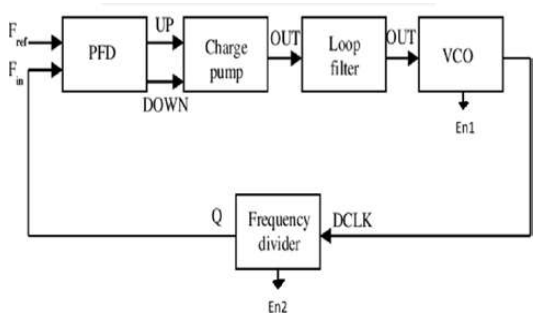

Figure 3 General architecture of Configurable PLL

Figure 4 represents schematic of Phase frequency detector and on right Charge pump. In order to reduce disturbances at the input of the voltage controlled oscillator (VCO) and obtain a smoother and sharper signal at the output, a charge pump circuit and low pass filter are employed [9]. The phase detector [5] is designed using positive edge triggered D flip flop along with reset, a reference frequency(Ref) is given at the input along with the feedback signal (V) from the VCO. Phase detector compares both the signals and gives respective up signal or down signal based on whether the frequency of the VCO has to be increased or decreased. The schematic of the PFD is as shown in Fig.4 (Left). The outputs, up and down signals are sent to the charge pump where voltage conversion takes place using the charges stored in the capacitors.

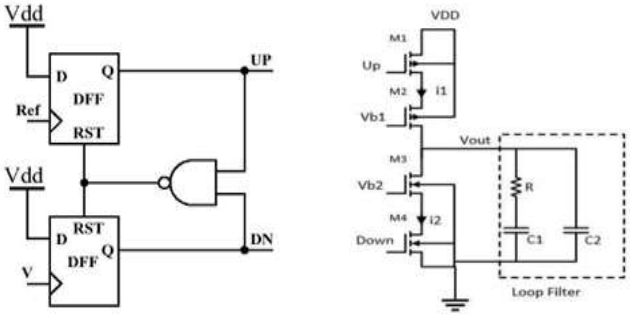

Figure 4 Schematic of Phase frequency detector (left) and Charge pump (Rt)

The designed PLL architecture includes two enable signals, En1 and En2. En1 determines the number of stages in the VCO, while En2 controls the frequency division of the feedback signal. By combining these two enables, four different PLL configurations can be achieved, each with a distinct frequency range.

The frequency range of the PLL is thus controlled by En1 and En2. Table I provides the various enable inputs and the corresponding PLL structure for each condition.

Table 1 Configurations of PLL

PLL CONFIGURATIONS		
En1	***En2***	***Structure of PLL***
0	0	14 stage VCO with Frequency Division
0	1	14 stage VCO without Frequency Division
1	0	4 stage VCO with Frequency Division
1	1	4 stage VCO without Frequency Division

3. SIMULATION RESULTS

When En1 is enabled, the VCO operates as a 14-stage VCO, but when En1 is disabled, it functions as a 4-stage VCO. The variation of frequency with respect to the voltage is shown in TABLE I for both 4 staged and 14 staged VCO.

Table 2 Frequency Range of VCO

VOLTAGE (Volts)	FREQUENCY	
	4 stage VCO (GHz)	14 stage VCO (MHz)
0.8	1.35	295.0
0.9	1.36	295.2
1.0	1.374	295.9
1.1	1.392	297.0
1.2	1.42	303
1.4	1.44	326

The proposed design has been implemented in Cadence, Virtuoso and simulated to test and verify its working. Figure 6 gives screenshot of one of the locked frequency of the implemented configurable PLL.

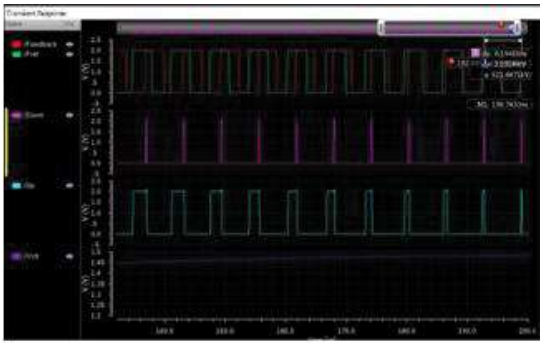

Figure 6 Phase locking of the PLL at lowest frequency

Phase Locking Time of the PLL when both En1 and En2 are high and PLL is working with 14 staged VCO connected to a Frequency divider, this configuration gives the lowest possible frequency of operation. It is found that for the reference frequency of 150 MHz, the Phase Locking period is 198.7433 ns.

4. CONCLUSION

A new approach to configurable architectures for chip design for PLL has been presented which makes it possible to configure the frequency range for wide range just by varying two signals En1 and En2. This enables frequency changes in a PLL without modifying the design at its core. These signals control the number of stages in the VCO and the frequency division of the feedback signal, thereby regulating the operating frequency range of the PLL. The number of stages in the sub-VCO and main VCO is determined based on the required frequency, which governs the PLL's operation within that

frequency range. For higher frequencies, the sub-VCO is not utilized. For lower frequency applications, the number of stages in the sub-VCO is determined and added to increase the overall number of VCO stages. This approach allows for flexible operation of the PLL across various frequency ranges without needing to reconfigure the core design.

5. REFERENCES

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