# Design of Power Efficient 14T Full Adder Circuit

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**ABSTRACT**

***Power-aware design is a continuously developing trend in VLSI that contributes to energy efficiency in battery-energized systems, electromechanical devices using semiconductors, and electronic components. In very simple terms, an adder is so important in arithmetic logic units. There are many approaches that researchers have considered to optimize the design of a full adder. This paper proposes an inventive and effective 14T power-efficient full adder circuitry. The proposed design bases mainly on the NMOS logic or Pass Transistor Logic (PTL), whose alternative implementation could also be done using transmission gates. The full circuit has been developed on the schematic as well as layout level using the Microwind EDA and DSCH3 tools, specifically focusing on power efficiency at the summation output node and carry output node. Performance evaluation in relation to an existing 14T adder design has shown drastically lower energy consumption.***

**Keywords:**

***VLSI (very large scale integration), EXOR gates, MOS transistor, layouts, microwind, DSCH3***

## 1. INTRODUCTION

This project introduces a new method of designing an energy-efficient full adder for application in energy-limited systems, like battery-operated systems and electronic devices. A full adder is an essential component of arithmetic logic units (ALUs) that performs binary addition, and its design must be optimized in order to maximize overall energy efficiency in digital circuits[1][6]. The design uses a 14-transistor (14T) based on NMOS logic or Pass Transistor Logic (PTL) and an alternative implementation with transmission gates[2]. The method specifically targets minimizing both summation node and carry output node power consumption, which are among the most influential determinants of overall energy efficiency in the adder[3][5]. The circuit is designed at both schematic and layout levels with the help of Microwind EDA and DSCH3 tools, enabling precise simulation and analysis. Compared to the current 14T adder designs, the new circuit exhibits a high level of reduction in energy consumption, thus a more power-efficient solution for power-constrained applications in VLSI systems[4]. This innovation helps solve the need for low-power designs in current electronic devices. For reducing the transistor count we use CMOS transistors but they are need to modified to a technology called Gate diffusion input (GDI), Transmission gate logic (TGL) and pass transistors logic (PTL)[1][13]. These techniques can reduce transistor count and power consumption. However we use FinFet technique to improve the speed up to 40% and also it will be supplement in reducing power consumption [2-3][8].

FinFET technology, whose emergence in recent years has revolutionized the art of low-power circuit design by alleviating the inadequacies of traditional planar CMOS transistors. FinFETs exhibit better electrostatic control over leakage currents and switching efficiency because of their three-dimensional structure. Thus, they are very good candidates to be adopted in the design of power-efficient arithmetic circuits such as full adders, where the minimization of transistor count and power consumption is paramount [10]. By combining FinFETs with advanced design techniques, such as Gate Diffusion Input (GDI) and Pass Transistor Logic (PTL), the modern full adder circuits have taken a significant stride towards the reduction of dynamic and static power dissipation [14]. These advances will immensely benefit their applications in mobile computing, IoT devices, and high-speed processors, where energy efficiency is a key design challenge without degrading performance [7][9].

Table1: Performance Analysis of 28T Full Adder

| Voltage supply(V) | Conventional(pA) | Usvl (pA) | Lsvl (pA) | Svl(pA) |
|---|---|---|---|---|
| 0.5 | 2.323 | 1.907 | 1.179 | 1.803 |
| 0.7 | 2.932 | 2.083 | 1.297 | 1.119 |
| 0.9 | 3.487 | 3.475 | 1.401 | 1.398 |
| 1.0 | 3.749 | 3.748 | 1.451 | 1.451 |
| 1.2 | 4.898 | 4.258 | 1.557 | 1.557 |

Table1 depicts the power used by 28t full adder and its performance. Our work will reduce the power concerns compared to 28t full adder.

## 2. RELATED WORKS:

### *2.1 Implementation and Installation Process*

***From The web***

- Open the page <ni2>
- Then connect to it
- Click<ni2>
- Click<ni2>
- *Test: click twice on MICROWIND3.EXE. Click "File ->Load", select "CMOS.msk". Click "Simulate"*

Click<ni2>

- get all the required projects in the chosen file.
- *Test: have a two time click on DSCH3.EXE.Load*

Once installation is completed, two directories are, one for MICROWIND3, one for DSCH3. In each directory, there is a subdirectory named html which holds help files.

### *2.2 The MOS device and analog simulation*

This chapter delves into the CMOS transistor, detailing its layout, static characteristics, and dynamic performance. It also explores the vertical dimensions of the device, along with a three-dimensional representation of the fabrication process.

***Logic values:***

Three logic figures 0, 1 and X (unknown) are described as follows

***Analogy Simulation***

This is illustrated in below image figure1 which shows the simulation of a MOS device and its output at different levels. If the gate voltage is set to zero, then no channel is created thus disconnecting the source node. A combination thereof is differentially bypassed and allowed to pass merely when a positive voltage is applied at the point of the gate, Vg. It is unique to note that the NMOS device does a low conduction state at high gate voltages during the non- conducting modes. Furthermore, upon reaching Vdd = 0.85V, V_NMOS=V_DD-Threshold. The NMOS devices do not function efficiently with a high gate voltage (logic 1) as is seen from the figure. One can run other such simulations also by clicking "More" or opening the editor window.

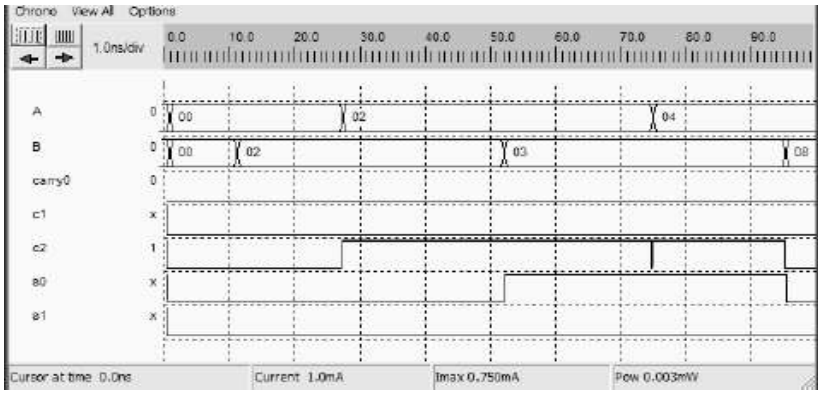


Figure 1: Simulation of MOS Device

Microwind is a nanometre-scale IC simulation and design tool that enables circuit designers to create, visualize, and analyse the performance of integrated circuits under real operating conditions. Microwind helps save time and cost on the paper by facilitating the design of the IC before actual manufacturing and testing.

## 3. IMPLEMENTATION IN THE TOOLS

### *3.1 Full-Adder in DSCH3*

DSCH3 is another very popular tool for digital integrated circuit (IC) design, particularly for educational design. It forms part of a set of tools designed to give a straightforward and efficient means to design and simulate digital circuits. DSCH3 is generally used for digital circuit design, logic synthesis, and simulation, and it enables designers to construct, analyse, and test logic circuits in an intuitive environment.

***Simulation:*** DSCH3 has integrated simulation capabilities. It supports functional simulation (in order to test that the logic works as planned) and timing simulation (so that the design adheres to certain time specifications). The software tool offers simulation of the digital logic's behaviour over time, allowing users to experiment with how the circuit responds to various input combinations.

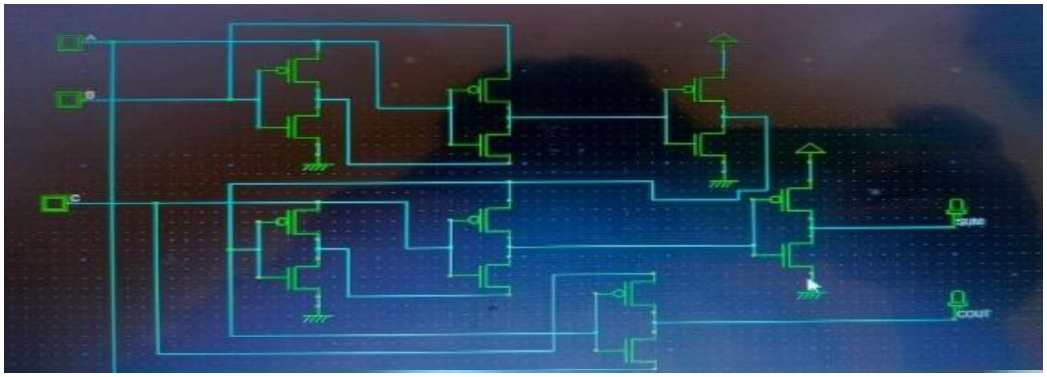

Figure 2: DSCH3 Schematic(The outline of the intended design 14T full adder)

### *3.2 Full Adder in Microwind*

Microwind is a layout and simulation software mostly employed for integrated circuit (IC) layout and verification, specifically in the area of VLSI (Very Large Scale Integration) design. It's an easy-to-use software package with both layout editing and simulation functionality that assists designers in designing, testing, and verifying the IC designs' functionality, especially those related to CMOS (Complementary Metal-Oxide-Semiconductor) process technologies.

***Simulation*:** Simulation is one of the most important aspects of Microwind, as it can simulate the ICs' behaviour under various operating conditions. It contains a SPICE-based simulator which enables the electrical characteristics, i.e., voltage, current, power, and timing of the components of the design to be analysed.

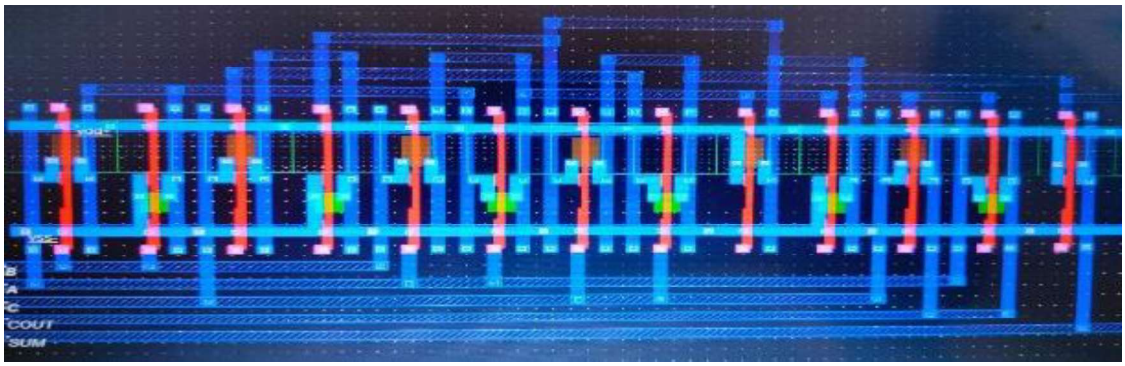


Figure 4: Microwind Layout

## 4. RESULTS AND DISCUSSION

The 14-transistor and 28-transistor full adders are simulated using the Microwind3 simulator. The power analysis from the simulation insightfully shows that the 14T full adder is more efficient than the 28T full adder in terms of power consumption. A comparison of both the adder designs in 180 nm technology is given in Table 2.

Table 2: Power consumption of 14T full adder

| Types of Adders | Static Power (nW) | | Dynamic Power (nW) | |
|---|---|---|---|---|
| Input1 | A=0, B=0, Cin=0 | | A=0, B=0, Cin=0 | |
| Operation | Sum | Carry | Sum | Carry |
| Proposed | 0.212 | 0.130 | 0.000 | 0.500 |
| Reference | 0.100 | 0.130 | 2.778 | 2.541 |
| Input2 | A=1, B=1, Cin=1 | | A=1, B=1, Cin=1 | |
| Operation | Sum | Carry | Sum | Carry |
| Proposed | 0.10 | 0.130 | 0.99 | 2.140 |
| Reference | 0.13 | 0.11 | 1.08 | 1.581 |

The summarized results highlight that the **14T full adder** demonstrates superior performance compared to the **28T full adder**. Reducing the transistor count significantly decreases power leakage, enhancing overall efficiency.

## 5. CONCLUSION

The current study describes a 14-transistor full-adder circuit that attains comparatively less power, less time of operation, and less density of transistors. Power optimization has been achieved in our full-adder design via structural modifications by applying concatenation techniques. Our circuit shows better results in terms of efficiency of transistors, area, and power consumption with very little distortion as compared to the currently available full-adder designs. Comparison with Table 1 shows that the 28T full adder consumes more power than the proposed design, which makes it efficient.

***Future Scope:***

- Power adaptation technique uses low-power VLSI design as future work that leads to advances in less power-consuming technologies by keeping power optimization strategies in focus.
- Reduction of transistor count to 12 using transmission gates could lead to a more energy-efficient circuit design.

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