Optimized 64-Bit Carry Select Adder Using Enhanced Full Adder for Reduced Power and Delay

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Abstract.

We aim to design an approximate 64-bit Carry Select Adder (CSA) by enhancing the full adder using a Look-Up Table (LUT) structure. In today's digital world, where nearly everything relies on digital chips, electronic adders play a crucial role in performing arithmetic operations within these systems. Although many techniques already exist, we propose a novel method for constructing a CSA. Our approach utilizes an improved full adder design incorporating multiplexers (MUX) to minimize power consumption, area usage, and propagation delay.

Keywords. Binary to Excess-1 Converter (BEC), Ripple Carry Adder (RCA), Electronic Adder, Power Minimization, Delay Minimization.

1. INTRODUCTION

Fast and efficient binary addition is the main business of CSAs, which makes them essential for digital arithmetic devices. However, there are many difficulties in conventional designs for reducing power and delay, with 64-bit technologies being the worst hit. This paper proposes an Efficient 64-bit Carry Select Adder in Enhanced Full Adder (EFA)-based architecture to achieve lower delay and power consumption by reducing redundant calculations. With growing digital demands, there is a need for speed and efficiency in circuit design. Our proposed adder improves the performance aspect and thereby offers a good solution for modern digital systems.

2. Existing and Proposed Models

2.1 Existing Solution

For arithmetic operations, digital circuits are very important; some types of adders are ripple, full, and carry select adder (CSA). However, these earlier adders fall short of being scalable and efficient, especially when performing large-bit operations. Full adders are not efficient for high-bit operations while parallel adders have delays that depend on the size of the bits. Carry look-ahead adders are fast but complicated; CSAs are also fast but cannot be stretched after a certain limit. Since this delay in full adders dictates how a CSA functions, much- needed improvement designs are made here.

2.2 Proposed solution

We have restructured the entire full adder switching of MUX and universal gates for better efficiency. The most significant minimization of delays in the circuit is to use pass

transistor logic. A 2:1 MUX has been included to optimize sum and carry computation, using carry input selection signal. This state application can also be sped up with lowered power consumption. The proposed solution greatly enhances the digital circuit operation.

We redesigned the complete full adder using MUX and universal gates to improve efficiency. The circuit was minimized to the greatest extent in terms of delays using pass transistor logic. A 2:1 MUX was incorporated to optimize sum and carry computations, using carry input as a selection signal. This, too, speeds up the operation and reduces power consumption. The suggested solution stands to make great improvements in the everyday application of digital circuits.

Cin	A	B	Sum		Carry	
0	0	0	0	XOR	0	AND
	0	1	1		0	
	1	0	1		0	
	1	1	0		1	
1	0	0	1	XNOR	0	OR
	0	1	0		1	
	1	0	0		1	
	1	1	1		1	

Figure 1:Truth Table of Full Adder

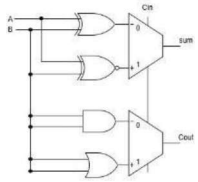

Figure 2:: Full Adder

3. COMPARISION OF EXISTING AND PROPOSED METHODS

DESCRIPTION	PROPOSED METHOD (64 bit)	EXISTING METHOD (32 bit)
Area(microM^2)	404	2315
Delay(ns)	3.252	3.4
Power(microW)	20.40	23.58

Figure 3:Comparision Table

4. ADDER

Designing the 64-bit Carry Select Adder (CSA) is structurally distinct from a traditional CSA. It is not an automatic synthesizer but is intended to optimize the carry chain carefully for better efficiency. The outputs of the full adders are fed into a multiplexer, where the final output of the Carry Select Adder (CSA) is determined based on the input carry signal. MUX output is thus dependent on the select input for faster computation. This optimized architecture provided improvements in speed and power savings across traditional CSAs.

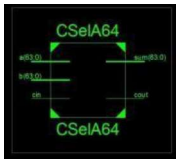

Figure 4:Schematic of CSA

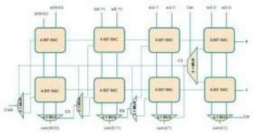

Figure 5:Block diagram of CSA

5. LAYOUT RESULTS

The 64-bit CSA design works by reducing carry propagation delay through parallelization, thus enhancing its speed and efficiency. This layout infers circuit complexity while optimizing the performance as well as power consumption.

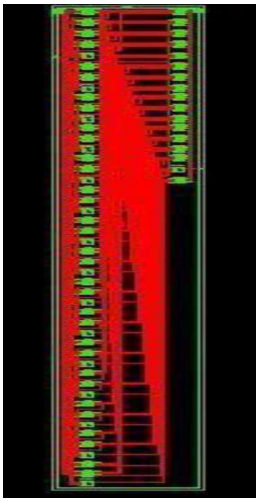

Figure 6:RTL schematic Diagram Schematic

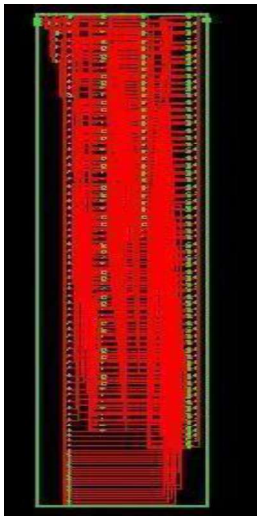

Figure 7:View Technology

Partitioning Into Smaller Blocks:

- That's broken down into sub-blocks; e.g., four 16-bit blocks of a 64-bit addition.
- This partitioning permits the partial results to be computed concurrently.

Basic Adders:

- To compute the sum, each block utilizes two Ripple Carry Adders (RCAs): ▪ One for 0 carry-in(one RCA assumes the carry-in is 0). The other RCA takes carry-in as1 **Multiplexers (MUXes):**
- Each block contains a 2:1 multiplexer to select the right sum and carry out.
- The one that selected is the real carry-in signal to the block, depending on the previous block carry out.

Hierarchical Carry Propagation:

- Not the previous block carry-out, but one block carry-out serves as to be carry-in for the next one.

Control Logic:

- The control logic synchronizes the carry signals and the sums through the multiplexer network.

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RTL Schematic Depiction:

- Four such smaller blocks (like 16-bits each) will be arranged side by side.
- Two RCAs to compute the parallel sum in each block.

6. SIMULATION RESULTS

In the simulation results, the proposed technique shows less delay than the conventional CSA. Below is the simulation response (first and second configuration) for validating the design

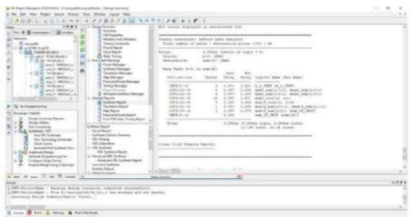

Figure 6: Simulation results in Xilinx ISE

Figure 7: simulation results in model Sim

7. FUTURE SCOPE

This proposed design increases flexibility due to area reduction due to fewer gates. The proposed method can be extended to the future scope of 128 bit.

8. CONCLUSION

The proposed optimized 64-bit carry select adder (CSA) incorporating an enhanced full adder design effectively achieves significant reductions in both power consumption and propagation delay compared to conventional architectures

9. REFERENCE

1. **Bhattacharjya, B., Maity, B., & Dutt, N. (2023).** ***Locate:*** *Low-Power Viterbi Decoder Exploration using Approximate Adders*. arXiv preprint arXiv:2304.03257, April 2023.

2. **Sharmila Devi, S., Karthikeyan, S., Abinaya, M., Kiruthika, V., & Adline Jancy,** Y. (2024). *Enhanced Low Power Carry-Select Adder using Transmission Gate Logic*. Journal of Electrical Systems, 20(9s), 1–8, June 2024.

3. **G. Kaur, L. Kaur, and N. Kaur,** "Reduced area carry select adder with low power consumption," *International Journal of Emerging Engineering Research and Technology*, vol. 3, no. 3, pp. 90-95, Mar 2015.

4. **Balasubramanian, D. L. Maskell, and N. E. Mastorakis,** "Speed and Energy Optimised Quasi-Delay-Insensitive Block Carry Lookahead Adder," *arXiv preprint arXiv:1903.09433*, Mar. 2019

Biographies

Mr Sankara RAO Allada, post graduate in Vlsi System Design engineering and pursuing phd in the area of Wireless sensor networks.Currently he is an Assistant professor in the department of ECE at Dadi institute of engineering and technology.He has over 13 years of teaching experience in microprocessors, electronics and communication based subjects.Areas of interest include,Digital image processing,signals and systems,Internet of things and Vlsi related coding.

Dr. B. Anjanee Kumar is an Associate Professor, Dadi Institute of Engineering and Technology, Anakapalle, Andhra Pradesh. He is currently handling a wide range of administrative and academic duties. He received his Ph.D. from NIT Warangal, where he completed a thesis titled "Optimization of Novel Design Architecture for Enhancement of Lifetime in Battery-Limited Sensor Nodes." With eight years of teaching experience at leading institutions, he has built a strong reputation as a knowledgeable and dedicated educator.He has delivered numerous expert sessions on ethical hacking and internet security for both student and faculty forums.

He has numerous journal publications to his credit and has presented over 40 papers at national and international conferences. He serves on the editorial boards of various peer- reviewed journals and books, and is also an invited reviewer for several internationally reputed journals.

Kandregula Jyoshna, Kirla Pravallika, Medisetti Chandrasekhar and Konathala Venkat are final yearBachelor's students in Electronics and Communication Engineering at Dadi Institute ofEngineering and Technology. Jyoshna is an ambitious learner focused on innovation and excellence. Pravallika is dedicated to applying her technical skills to realworld challenges. Chandra Sekhar and Venkat is eager to grow and contribute to the field through continuous learning. Together, they strive to enhance their knowledge and make a meaningful impact in the engineering domain.