Analysis of Quasi-Coaxial Via Implemented in IC Substrate using Multiple-Scattering Method

Hiroaki Takahashi, Pelin Suealp, and Erich Schlaffer

Abstract—**This paper presents an analytical study of a quasi-coaxial via implemented in an IC substrate using the multiple-scattering method. The plate-via impedance matrix is derived using addition theorems for cylindrical inward and outward waves around the vias. This matrix is then utilized to determine the loop inductance, taking into account the via-barrel radius. The derived equations facilitate the investigation of loop inductance, which serves as a figure of merit for the quasi-coaxial configuration. Additionally, the paper includes a statistical analysis that accounts for design parameter uncertainties from via manufacturing point of view.**

Index Terms—**Via modeling, quasi-coaxial via, multiple-scattering method, loop inductance**

I. INTRODUCTION

Wireless communication with high data rates is the indispensable infrastructure for cutting-edge technologies such as artificial intelligence, machine learning (ML), virtual reality, quantum communication, quantum ML, blockchain, THz-sensing, and edge computing [1]. To fulfill the increasing demand for fast and low-latency communication, millimeter-wave bands are available with the launch of the 5G New Radio based on advanced semiconductor technologies. Further enhancement in network infrastructure with the concept beyond 5G/6G seeks for the possible use of communication using frequencies above 100 GHz as D-band (110–170 GHz) shows great potential and is being investigated for emerging future wireless communication technologies [2].

Advanced packaging technologies play a crucial role in the next generation of wireless communications. In the early stages of the chip and antenna design phases, packaging systems have to be co-developed and tested as it is critical due to the challenges of system integration [3]. To increase the degree of integration density for electrical interconnections, embedding technologies have been proposed and demonstrated. For instance, the so-called center core embedding presented in [4] uses organic IC-substrates or printed-circuit boards (PCBs) to place active and passive components inside the structures. The embedding of multiple components can be realized through panel-level technologies with chip-first embedding or chip-last assembly. This contributes to the further small footprint, high mechanical stability, and reliable copper interconnections without soldering as shown in Figure 1.

Regarding electrical performance, ohmic losses derived from lossy dielectric material and conductor material with

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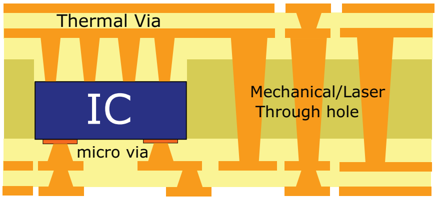
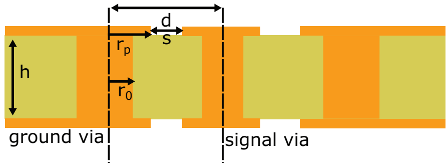
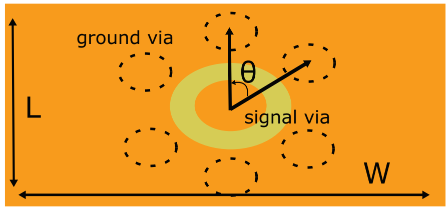


Fig. 1. Stack-up of a center core embedding with different via interconnections: microvia, thermal via, and mechanical/laser through hole.



(a)



(b)

Fig. 2. Cross-section of quasi-coaxial via: (a) xz-plane; (b) xy-plane.

finite conductivity increase at higher frequencies. On the other hand, inductive and capacitive parasitic effects significantly impact signal integrity at higher frequencies. These parasitic effects are introduced at discontinuities, which are common in complex IC packages. Such discontinuities occur at curves, bends, and, most notably, vertical interconnections involving via structures. Vias enable vertical interconnections across IC substrates, from embedded chips to PCBs. However, without careful design, it can lead to significant degradation of electrical performance.

The electrical behavior of via structures has been investigated from an electromagnetic compatibility perspective through both theoretical and experimental approaches. A vast amount of hybrid field-circuit via modeling has been previously presented [5]–[11]. A via located within a parallel conductor plate can be seen as equivalent to a radial waveguide with transverse magnetic modes to propagation direction z, denoted as TM^z_{mn} [10]. Moreover, the currents flowing at the surface of a via barrel cause the no-cutoff parallel plate propagation wave and evanescent waves between the via and the plate contributing to the increase of the reactance [7]. The excitations can result in additional loss, reflection, and unwanted coupling to other signal lines. To improve signal integrity at the vertical interconnection, multiple ground vias surrounding the signal via can be utilized to suppress spurious emissions and undesired reflections [12], which is named quasi-coaxial via. The authors in [13] and [14] demonstrated the analysis of the loop inductance derived from the quasi-coaxial via based on an analytical inductance formula or physics-based via modeling approach. The loop inductance should be a figure of merit to clarify the frequency-dependent performance of quasi-coaxial via. In this study, we exploited the multiple-scattering method presented in [5] and [6] for the loop inductance analysis to take the via barrel radius into account, which is ignored in the previous studies. Furthermore, statistical analysis of the loop inductance based on the manufacturing capability of vias implemented in a typical IC substrate is also presented. The structure of the paper is as follows:

Section II briefly explains the theory behind the study, the extraction of loop inductance of via, and the calculation of via plate impedance matrix using the multiple-scattering method. Section III demonstrates the loop inductance analysis based on several cases of quasi-coaxial via as well as statistical analysis from the manufacturing point of view, which is followed by the conclusion in Section IV.

II. THEORY

In this section, the structure to be analyzed is introduced, and the procedure for the extraction of loop inductance and the derivation of plate via impedance matrix using the multiple-scattering approach are introduced. The structure to be analyzed is shown in Figure 2. Quasi-coaxial via consists of a signal via and surrounding ground vias. Design parameter is the following: the via barrel radius r_0, the via pad r_p, the distance to the edges s, total pitch d, and the height of the dielectric layer h. Due to the ease of theoretical derivation, the dielectric layer is assumed to be homogeneous over the domain of interest with identical relative dielectric constant, ε_r or Dk, and loss tangent, tanΔ or Df.

For signal integrity analysis of the quasi-coaxial via structure, the concept of the plate via impedance matrix denoted as $\mathbf{Z}_{\mathrm{PP}}$ is used, which is formulated in

$$\mathbf{V} = \mathbf{Z}_{pp}\mathbf{I}, \tag{1}$$

where $\mathbf{V} = [V_1, V_2, \ldots, V_{\mathrm{P}}]^T$, and $\mathbf{I} = [I_1, I_2, \ldots, I_{\mathrm{P}}]^T$. P is the number of vias including signal via and ground vias. This P × P matrix relates the voltage of a via to the current of the via and the others. Ground vias are defined as the via shorted to the ground plate, i.e., $V_i = 0$. According to [13] and [14], the plate via impedance matrix $\mathbf{Z}_{\mathrm{PP}}$ can be converted into the loop inductance matrix denoted as $\mathbf{L}_{\mathrm{Loop}}$ depending on the number of signals and ground vias.

A. Extraction of Loop Inductance

Although the conversion method is detailed in [13] and [14], the mathematical procedure is briefly explained as follows: To determine the loop inductance matrix $\mathbf{L}_{\mathrm{Loop}}$, we exploit the imaginary part of the via-plate impedance matrix, $\mathbf{Z}_{\mathrm{PP}} = \mathbf{R} + j\omega\mathbf{L}_{\mathrm{PP}}$ as

$$\mathbf{V} = j\omega\mathbf{L}_{\mathrm{pp}}\mathbf{I}. \tag{2}$$

To derive the loop inductance, the plate via inductance matrix is decomposed into blocks, namely signal inductance matrix $\mathbf{L}_{\mathrm{SS}}$, ground inductance matrix $\mathbf{L}_{\mathrm{GG}}$, and signal-ground matrix $\mathbf{L}_{\mathrm{SG}}$ and $\mathbf{L}_{\mathrm{GS}}$ as shown below.

$$\begin{bmatrix} \mathbf{V}_S \\ \mathbf{V}_G \end{bmatrix} = j\omega \begin{bmatrix} \mathbf{L}_{\mathrm{SS}} & \mathbf{L}_{\mathrm{SG}} \\ \mathbf{L}_{\mathrm{GS}} & \mathbf{L}_{\mathrm{GG}} \end{bmatrix} \begin{bmatrix} \mathbf{I}_{\mathrm{S}} \\ \mathbf{I}_{\mathrm{G}} \end{bmatrix}, \tag{1}$$

where $\mathbf{V}_S = [V_1, V_2, \ldots, V_S]^T$, and $\mathbf{V}_G = [V_{S+1}, V_{S+2}, \ldots, V_G]^T$, as well as $\mathbf{I}_S$ and $\mathbf{I}_G$. Taking the inverse of the inductance matrix $\mathbf{L}^{-1} = \mathbf{B}_{\mathrm{PP}}$ and considering the relation between signal and ground vias, i.e., $\Sigma_{i=1}^{S} I_i = -\Sigma_{j=1}^{G} I_j$, the dimension of the matrix can be reduced from P × P to (S + 1) × (S + 1) as follows:

$$\begin{bmatrix} \mathbf{B}_{\mathrm{SS}} & \mathbf{B}_{\mathrm{SG}}\mathbf{e}_{\mathrm{G}} \\ \mathbf{e}_{\mathrm{G}}^T\mathbf{B}_{\mathrm{GS}} & \mathbf{e}_{\mathrm{G}}^T\mathbf{B}_{\mathrm{GG}}\mathbf{e}_{\mathrm{G}} \end{bmatrix} \begin{bmatrix} \mathbf{V}_S \\ V_G \end{bmatrix} = j\omega \begin{bmatrix} \mathbf{I}_S \\ I_G \end{bmatrix} \tag{3}$$

where $\mathbf{e}_G$ is the $G \times 1$ column vector whose entries are all ones. Taking inverse of eqn (3), we can obtain the equivalent inductance matrix $\mathbf{L}_{\mathrm{eq}}$, from which the loop inductance matrix $\mathbf{L}_{\mathrm{Loop}}$ is calculated,

$$\begin{bmatrix} \mathbf{V}_S \\ V_G \end{bmatrix} = j\omega \begin{bmatrix} \mathbf{L}'_{SS} & \mathbf{L}'_{SG} \\ \mathbf{L}'_{GS} & \mathbf{L}'_{GG} \end{bmatrix} \begin{bmatrix} \mathbf{I}_S \\ I_G \end{bmatrix} \tag{3}$$

$$\mathbf{L}_{\mathrm{Loop}} = L_{SS} - L_{SG}\mathbf{e}_G^T - \mathbf{e}_s L_{GS} + L_{GG}\mathbf{e}_G\mathbf{e}_S^T \tag{4}$$

where $\mathbf{e}_S$ is the $S \times 1$ column vector whose entries are all ones.

B. Multiple-Scattering Method

As formulated, the loop inductance of quasi-coaxial vias is extracted from the via-plate impedance matrix $\mathbf{Z}_{PP}$. This indicates that the accuracy of the analysis depends on that of the calculation for $\mathbf{Z}_{PP}$. There have been several methods proposed to determine Z_{PP}, such as physics-based via modeling [7], intrinsic via modeling [9], and multiple-scattering method [5], [6]. The multiple-scattering method enforces the boundary conditions at the surfaces of via barrels and takes the electromagnetic field interactions between vias in the parallel plate propagation mode and evanescent modes into account. A quasi-coaxial via is supposed to have electrical characteristics dependent on their geometry and relative location between signal via and ground vias. Thus, the multiple-scattering method is employed for rigorous analysis. In the original multiple-scattering method, one needs to solve the Foldy–Lax equation including complicated Green's functions. The theory is reformulated by Zhang et al. in [6] to a simplified form and the mathematical procedure for Z_{PP} is briefly explained as follows:

The method considers the wave distributed around an ith via and the parallel plate decomposed into an infinite summation of modes as below

$$\mathbf{E}_Z^{(i)} = \sum_{m=-\infty}^{\infty}\sum_{n=0}^{\infty}\begin{Bmatrix} b_{mn}^{(i)}(\rho^i,\phi^i,z) \\ +a_{mn}^{(i)}J_{mn}^{(i)}(\rho^i,\phi^i,z)\end{Bmatrix}, \tag{4}$$

where ρ^i, ϕ^i, z are cylindrical local coordinates of an ith via, and $b_{mn}^{(i)}$ and $a_{mn}^{(i)}$ are the mode expansion coefficients of outward and inward cylindrical harmonics, respectively. It is worth mentioning that the dielectric layer thickness should be enough small that TE_{mn}^{z} modes can be ignored. The cylindrical harmonics $H_{mn}^{(i)}$ and $J_{mn}^{(i)}$ are respectively described as

$$J_{mn}^{(i)}(\rho^i,\phi^i,z) = J_m(k_n\rho^i)e^{jm\phi^i}\cos\left(\frac{n\pi}{h}z\right) \tag{5}$$

$$H_{mn}^{(i)}(\rho^i,\phi^i,z) = H_m^{(2)}(k_n\rho^i)e^{jm\phi^i}\cos\left(\frac{n\pi}{h}z\right), \tag{6}$$

where k_n is the effective wavenumber, i.e., $k_n = \sqrt{\varepsilon_r k_0^2 - \left(\frac{n\pi}{h}\right)^2}$, and $J\,(\cdot)$ and $H_m^{(2)}(\cdot)$ are the mth-order Bessel function of the first kind and mth-order Hankel function of the second kind, respectively. As detailed in [9], the accuracy of the analysis depends on the truncated number M for the azimuthal component and N for the axial component. When n equals to zero, the no-cutoff parallel plate propagating wave can be taken as the wave scattered at each via, whereas evanescent waves are considered with $n \geq 1$. In this study, m is always zero because the distance between vias is so large due to the constraint by the laser via the manufacturing process that higher-order azimuthal components can be ignored. Considering the mathematical assumptions above, one can reformulate the equation of E_z and based on Maxwell's equations, $H_\phi(\rho^i, \phi^i, z)$ can be also derived as

$$H_\phi^{(i)} = \sum_{n=0}^{N}\frac{j\omega\epsilon}{k_n}\begin{bmatrix} b_{0n}^{(i)}H_1^{(2)}\left(k_n\rho^i\right) \\ +a_{0n}^{(i)}J_1\left(k_n\rho^i\right)\end{bmatrix}\cos\left(\frac{n\pi}{h}z\right). \tag{7}$$

Therefore, the total magnetic field around quasi-coaxial via is described as

$$H_\phi(r,\phi,z) = \sum_{i=1}^{P}H_\phi^{(i)}(\rho^i,\phi^i,z). \tag{8}$$

The inward mode expansion coefficients of each via, $a_{0n}^{(i)}$ are included in the mode expansion coefficient vectors $\mathbf{a}_{0n} = [a_{0n}^1, a_{0n}^2, \ldots, a_{0n}^P]$ as well as $b_{0n}^{(i)}$. According to [9], the mode expansion coefficient vectors can be determined by addition theorems of cylindrical waves, including both the zero-order propagating and the higher-order evanescent modes as

$$\mathbf{a}_{0n} = \left(\mathbf{I} - \mathbf{S}_{PP}^{R}\Gamma\right)^{-1}\left(\mathbf{a}_{en} + \mathbf{S}_{PP}^{R}\mathbf{b}_{en}\right) \tag{9}$$

$$\mathbf{b}_{0n} = \Gamma \mathbf{a}_{0n}, \tag{10}$$

where $\mathbf{a}_{en}$ and $\mathbf{b}_{en}$ represent the expansion coefficients of the initial inward and outward cylindrical waves derived from the excited TEM (Transverse Electromagnetic mode) at the excitation ports as

$$b_{en}\left(V_0, z'\right) = \frac{j\pi V_0}{h\ln r_p^i / r_0^i} \frac{\cos\left(\frac{n\pi z'}{h}\right)}{1 + \delta_{n0}} \left[J_0\left(k_n r_p^i\right) - J_0^{(2)}\left(k_n r_0^i\right)\right] \tag{11}$$

$$a_{en}\left(V_0, z'\right) = \frac{j\pi V_0}{h\ln r_p^i / r_0^i} \frac{\cos\left(\frac{n\pi z'}{h}\right)}{1 + \delta_{n0}} \left[H_0\left(k_n r_p^i\right) - H_0^{(2)}\left(k_n r_0^i\right)\right], \tag{12}$$

and $\mathbf{H}_0 = \text{diag}\left\{H_0^{(2)}(kr_i)h\right\}$, $\mathbf{J}_0 = \text{diag}\ \{J_0(kr_i)h\}$, $\mathbf{H}_1 = \text{diag}\left\{\frac{2\pi k r_i}{j\omega\mu} H_1^{(2)}(kr_i)\right\}$ $\mathbf{J}_1 = \text{diag}\left\{\frac{2\pi k r_i}{j\omega\mu} J_1(kr_i)\right\}$, $\Gamma_0 = \text{diag}\left[-\frac{J_0(k_n r_0^i)}{H_0^{(2)}(k_n r_0^i)}\right]$ and the element of $\mathbf{S}_{\text{PP}}^R$ can be calculated as

$$S_{\text{PP}}\left(i, j\right) = \left(1 - \delta_{ij}\right) H_0^{(2)}\left(k_n r_{ij}\right), \tag{13}$$

where r_{ij} means the distance between vias. Using the matrices above, the via plate impedance matrix derived from Multiple scattering method can be also formulated as

$$\mathbf{Z}_{\text{PP}}^R = \left(\mathbf{H}_0 + \mathbf{J}_0 \mathbf{S}_{\text{PP}}^R\right)\left(\mathbf{H}_1 - \mathbf{J}_1 \mathbf{S}_{\text{PP}}^R\right)^{-1}. \tag{14}$$

III. ANALYSIS

In this section, using the derived analytical equations in Sections II-A and II-B, the loop inductance of quasi-coaxial via dependent on the via geometry, the distance between vias, and the number of ground vias is investigated after the verification of analysis by comparison to the numerical simulation.

A. Verification of the Analytical Magnetic Fields

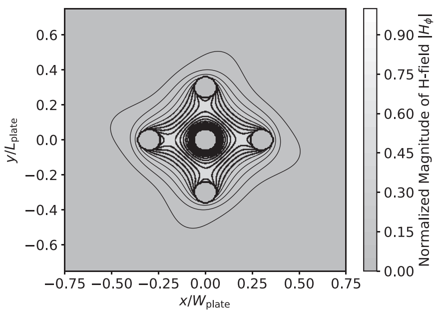
For verification of the analysis presented in the last section, the total magnetic field distribution $|H_\phi(r, \phi, z)|$ at 100 GHz around a quasi-coaxial via implemented in a homogeneous dielectric layer is calculated in Python/Julia environment and compared to the result of full-wave simulation. The dielectric material is assumed to be one of the typical materials for high-frequency IC-substrate, Panasonic LEXCMGX R-G545L, with Dk/Df of 3.6/0.002. Table 1 describes the parameters used for the analysis. Figure 3 shows the comparison in the normalized magnitude of magnetic fields between the equation and numerical simulation by CST Microwave Studio. Plot settings such as xy-range, scale, and contour levels are identical. The comparison shows a good agreement between the analysis and numerical simulation especially the H-fields with interaction between the signal via and ground vias by taking boundary conditions at via barrels rigorously into account.

B. Extraction of Loop Inductance of Quasi-Coaxial Via

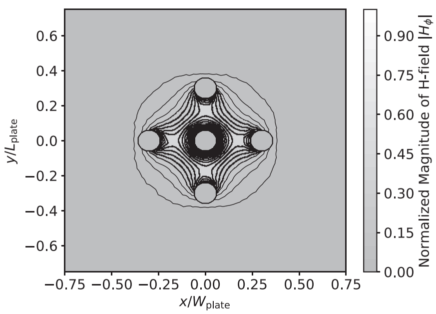
As mentioned earlier, the loop inductance of signal via and ground vias is a

TABLE 1
MATERIAL AND GEOMETRICAL PARAMETER OF QUASI-COAXIAL VIA

h, μm	t, μm	W, mm	L, mm	Dk	Df
100.0	12.0	2.0	2.0	3.6	0.02



(a)



(b)

Fig. 3. Contour plot of the magnitude of magnetic fields around a signal via and four ground vias at 100 GHz (a). Analytical calculation by eqn (7) and (8) with N = 3 (b) full-wave simulation (CST).

function of the via alignment. This is due to the variation of H-fields to the via locations. Previous studies in [9] and [14] showed the fact that the loop inductance can be decreased by making the distance of vias small so that the magnetic field can be confined within the domain of quasi-coaxial structure. For example, suppose a signal via as via1 located at the center of the same plate used in Section III-A surrounded by two ground vias, via2 and via3, with identical dimensions. The location of via2 is fixed above via1 on the same y-axis at a distance of 250 μm. The loop inductance L_{Loop3}, in this case, depends on the location of via3. Figure 4 shows the contour plot of the loop inductance as a function of the location of via3, which is normalized to the case only

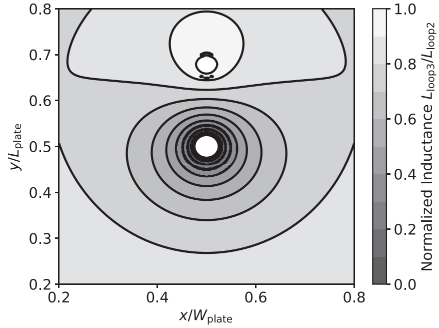


Fig. 4. Contour plot of normalized loop inductance of a quasi-coaxial via with three ground vias dependent on the location of the third ground via.

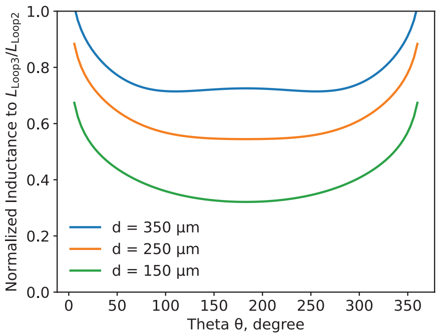
with via1 and via2 denoted as L_{Loop2}. The results suggest that the loop inductance varies with the position of via3 and can be reduced by positioning via3 closer to via1 and farther from via2. Similarly, Figure 5 illustrates the variation in loop inductance: (a) when the angle θ between two ground vias is varied at different distances from the signal via, and (b) when the distance from the signal via changes with different radii of the ground vias.

They implied that the loop inductance may be minimized when the distance between a signal via and ground vias is minimized and the distance between ground vias is maximized as well as the diameter of the ground vias.

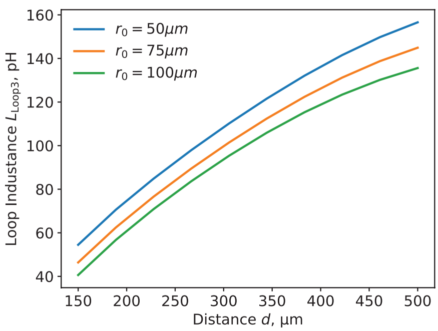
C. Statistical Analysis of Quasi-Coaxial Via

The analysis of quasi-coaxial via so far clarified how the design parameters affect the loop inductance of the structures. Moreover, from a practical manufacturing point of view, there are some considerations to improve the manufacturing reliability that constrains the design parameters as listed below:

1. The area of the via pad with radius r_p should be sufficiently large due to



(a)



(b)

Fig. 5. The calculated loop inductance with a single via and two ground vias with different design parameters: (a) the angle θ between two ground vias as shown in Figure 2(b) is varied between [0, 2π] with different distances to the signal via; (b) the distance to the signal via is varied with different radius of the ground vias.

the misalignment during the drilling and lamination process.

2. Misalignment of via hole depends on the drilling process mainly by laser drilling or mechanical drilling.
3. Laser via hole diameter needs to be enlarged as the dielectric layer thickness increases.
4. Despite the better fabrication accuracy of laser drilling compared to mechanical drilling, it still suffers from misalignment and fabrication uncertainty of via radius due to the factors such as mechanical property of a substrate material, plating

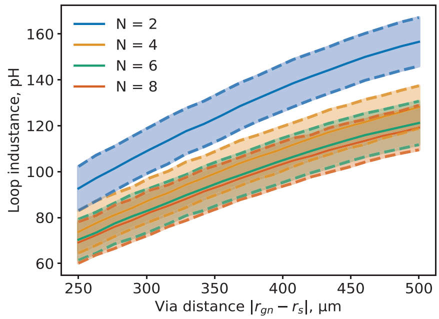


Fig. 6. The mean value of the loop inductance to the distance between a signal via and ground vias with different numbers of ground vias and their 95%- confidence interval of $2\sigma_L$ calculated from 1000 random Gaussian sampling based on input parameter variation $\sigma_r0 = 5$ μm and $\sigma_d = 5$ um

technology, lamination misalignment, laser focus adjustment, and pulse stability.

Therefore, statistical analysis that considers parameter uncertainties is essential for mass production. As mentioned earlier, the practical values of uncertainty parameters are highly dependent on the manufacturing process, drilling/plating technology, and dielectric material. In this study, the parameters with uncertainty include the via radius r_0, assumed to have a typical uncertainty of ±10 μm ($2\sigma_{r0}$) as well as the via distance d with ±10 μm ($2\sigma_d$). Figure 6 illustrates the loop inductance relative to the distance between a signal via and ground vias, incorporating various numbers of ground vias and including a 95% confidence interval calculated from 1000 Gaussian samples. As established in the previous section, the alignment of ground vias is symmetrical regardless of the number of ground vias present. The standard deviations of the loop inductance, σ_L, are 5.04 pH, 4.76 pH, 4.68 pH, and 4.69 pH when the number of ground vias is 2, 4, 6, and 8, respectively.

IV. CONCLUSION

This paper presented the analysis of quasi-coaxial via using the multiple-scattering method. The use of full-wave theory considering the inward and outward waves distributed via barrels by addition theorem enabled the rigorous calculation of plate-via impedance matrix. Afterwards, the derived equations were used for the study on the loop inductance of quasi-coaxial via dependent on the design parameters such as via radius, the distance between vias, and the their locations. Practical consideration in via manufacturing methods has been pointed out and, accordingly, statistical analysis was performed to figure out how the fabrication uncertainties can affect the loop inductance.

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