Advanced Substrate Technologies for Sub-THz Era

François Brunier

Abstract—**Electronic devices evolved significantly, driving the digital transformation toward a connected society. The increasing demand for performance, speed, and efficiency is pushing wireless applications to operate at sub-THz frequencies and beyond. Innovative substrates, such as fully depleted silicon on insulator (FD-SOI), indium phosphide on silicon (InPoSi), and SmartGaN, offer disruptive yet commercially viable solutions to efficiently utilize these frequencies. Achieving European leadership in these key markets requires establishing a complete and reliable supply chain from materials to applications. A so-called value chain model is applied in European KDT JU programs, which serves as a fast track to accelerate co-innovation and market adoption. This paper illustrates the innovation dynamics of the FD-SOI ecosystem in radio frequency applications up to 120 GHz, realized in the BEYOND5 project. It also explores technology disruption in the sub-THz frequency range by using InPoSi substrates in combination with the Smart Cut process. The Move2THz project aims to develop such technologies and demonstrate that it overcomes historical limitations of bulk InP. Finally, the paper demonstrates how the industry-proven Smart Cut technology can be adapted to other materials, such as gallium nitride, to complete the technological offering and meet market needs.**

Index Terms—**B5G, 6G, FD-SOI, mmWave, sub-THz, InP, InPoSi, Smart Cut, SmartGaN**

I. INTRODUCTION ON ADVANCED SUBSTRATES

IN collaboration with the Leti (French Laboratoire d'électronique et des technologies de l'information) Soitec developed the patented Smart Cut process over 30 years ago. This process, illustrated in Figure 1, enables to manufacture advanced substrates for microelectronics by transferring a thin active layer of silicon or another semiconductor material from a donor substrate onto a second substrate that acts as a support. This Smart Cut process ensures high yield and surface quality for industrial manufacturability. It facilitates scaling up wafer size and volume to align with complementary metal–oxide–semiconductor (CMOS) manufacturing capacities, minimizes the use of rare resources, reduces the technology's ecological footprint and cost, and offers a wide range of possibilities for material integration, as illustrated in Figure 2. The combination of an adapted active layer on a functional support substrate creates a more resilient and less dependent value chain.

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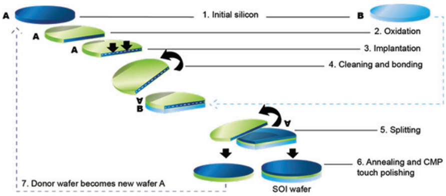

Fig. 1. Schematic illustration of the Smart Cut technology that manufactures SOI substrates.

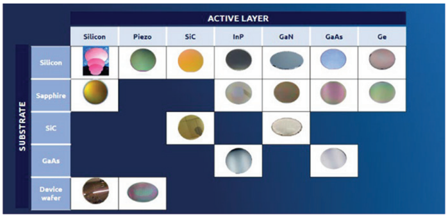

Fig. 2. Smart Cut technology combining an adapted active layer on a functional support substrate for a less dependent value chain.

II. RF TECHNOLOGY ON SOI – AN UNRIVALLED PPAC FOR 5G AND BEYOND

Radio frequency silicon on insulator (RF-SOI) and fully depleted silicon on insulator (FD-SOI) technologies based on SOI substrates meet the global 5G smartphone market requirements and offer new solutions for applications using the 5G frequency spectrum, ranging from low GHz bands to millimeter wave (mmWave) bands, including future prospects beyond 100 GHz. With its smaller device dimensions, FD-SOI enables very high cut-off frequencies, allowing circuit operations at very high frequencies, covering mmWave and beyond 100 GHz. The radio frequency front-end mmWave architecture, using a commercial low-leakage FD-SOI RF planar CMOS platform, has been successfully demonstrated in mobile market [1]. Additionally, FD-SOI allows co-integration of analog and digital capabilities into system-on-chip designs. Thanks to its back-biasing capability, FD-SOI also offers dynamic power/performance ratio tuning mechanisms. This makes FD-SOI also essential for automotive radar and Advanced Driver Assistance Systems (ADAS).

The KDT IA project BEYOND5, "Building the fully European supply chain on RF-SOI, enabling New RF Domains for sensing, Communication, 5G and beyond" leverages the RF-SOI and FD-SOI technologies to build a solid European ecosystem over different application domains. Started in June 2020, the project unites 39 European partners from 10 countries, covering the entire value chain with two SOI technologies (RF-SOI in STMicroelectronics, 22FDX in GlobalFoundries) and seven demonstrators. On the FD-SOI pilot line, GlobalFoundries develops and integrates new RF functions and reliability methodologies onto its 22FDX baseline. This includes the utilization of high resistivity base wafers to enhance the properties of 5G demonstrators and meet future mmWave system requirements.

This project's goal is to showcase these technology platforms at the system level. Figure 3 illustrates the consortium partners mapped onto the value chain, and Figure 4 depicts which technology platforms are incorporated in the different application demonstrators.

Each of the seven demonstrators selected the most competitive SOI technology based on its specific requirements,

Fig. 3. BEYOND5 project consortium partners mapped onto the value chain.

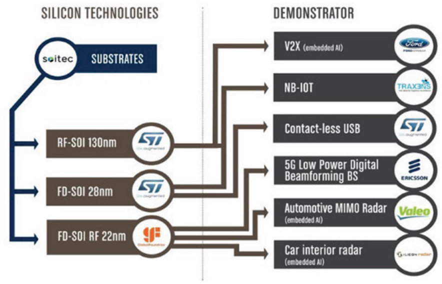

Fig. 4. BEYOND5 project demonstrators incorporate the different RF-SOI and FD-SOI technology flavor.

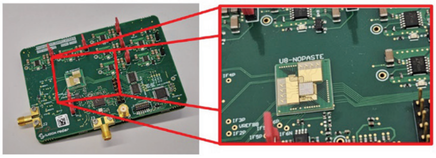

Fig. 5. 4 × 4 MIMO TRX 22FDX chip for the in-cabin radar demonstrator developed in the BEYOND5 project.

with key criteria including frequency range, performance, integration, power efficiency, and cost.

For the 122 GHz in-cabin radar and gesture recognition demonstrator, for example, the 22FDX was chosen for its RF performance, enabling low-power designs operating beyond 100 GHz. Its scaling effects facilitate true low-cost designs with minimal area consumption for processing units in system-in-package solutions. The in-cabin demonstrator, depicted in Figure 5, utilizes a 4 × 4 Multiple-Input Multiple-Output (MIMO) transceiver (TRX) chip with an in-package antenna operating in the 116–123 GHz band.

The block diagram of this millimeter-wave integrated circuit (MMIC) is illustrated in Figure 6. This TRX is developed using 22FDX technology from GlobalFoundries.

This 120 GHz MMIC shows exceptional performance in terms of noise figure (NF) and power consumption. The low-noise amplifier (LNA) achieves a NF of 6.5 dB and a gain of 14 dB in the relevant frequency band, illustrated in Figure 7.

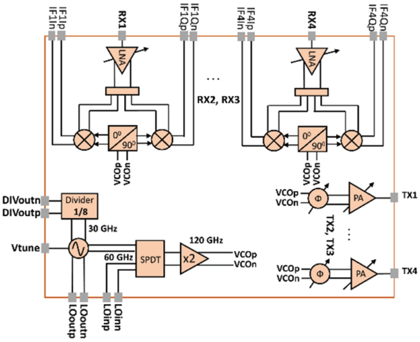

Fig. 6. The block diagram of the designed TRX for the in-cabin radar demonstrator developed in the BEYOND5 project.

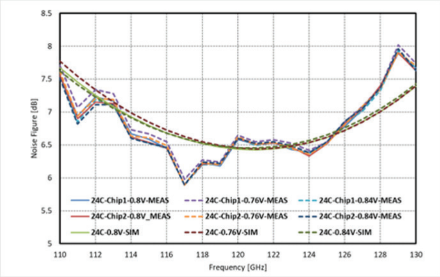

Fig. 7. TRX low-noise amplifier noise performance for the in-cabin radar demonstrator developed in the BEYOND5 project.

The MIMO 4 × 4 chip consumes a total of 260 mW during continuous operation, accommodating four receivers and one transmitter. The detailed performance metrics are given in Table 1.

III. SMART CUT ON III-V MATERIALS: INNOVATIVE SUBSTRATES FOR THz ERA

The Smart Cut process is also compatible with materials beyond silicon, reducing the reliance on rare and costly bulk materials, thus offering solutions for technological sovereignty aligned with the

TABLE 1.
THE MEASURED MIMO 4 × 4 CHIP PERFORMANCE.

Parameter	**120 GHz MPW2**
Frequency range	116–123 GHz
TX output power	3 dBm
Conversion gain RX	18 dB
RX noise figure	SSB: 9.1 dB
DC power consumption	260 mW (TX- 36 mW)

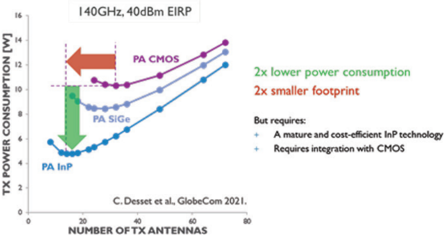

Fig. 8. Power consumption and footprint PA comparison across different technologies at 140 GHz operation frequency and 40 dBm effective isotropic radiated power.

Greendeal initiative. Indium phosphide (InP) offers exceptional capabilities that surpass other technologies in terms of performance and power consumption. It features superior power amplifier (PA) output power (P_{out}) and power added efficiency, along with low NF characteristic. Figure 8 compares PA performance and area metrics of competing technologies like CMOS, SiGe, and InP.

Despite its advantages, the InP technology faces limitations in reaching high-volume production markets primarily due to its manufacturing constraints, small diameters, and high costs. The Smart Cut process provides a sustainable and commercially viable solution for consumer applications like 6G mobile communication and high-resolution sensors. The Smart Cut process in combination with InP paves the way to increase the number of components from the same InP wafer by more than tenfold and to transition to larger wafer diameters using a tiling approach.

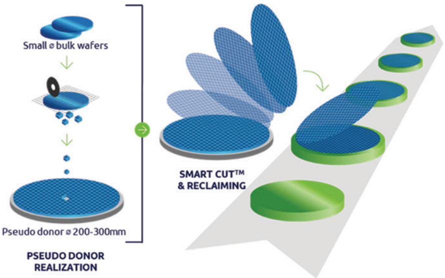

Fig. 9. Schematic of the Smart Cut with tiling approach.

The Smart Cut with tiling approach is illustrated in Figure 9. This approach involves arranging transferred layers on a larger substrate to optimize material usage and enhance production efficiency. On the left of Figure 9, the production of the pseudo-donor substrate through tiling is illustrated. On the right, the InPoSi substrate is shown, which is obtained from the pseudo-donor substrate via the Smart Cut process, demonstrating the concept of reclaiming the pseudo-donor substrate for multiple reuses.

The “Move2THz” KDT project, initiated on June 1, 2024, unites a European value chain of 28 partners specializing in InP technology development and application, as illustrated in Figure 10.

The Move2THz project aims to revolutionize the manufacturing process of InP platforms by establishing a groundbreaking global standard for InP on silicon (InPoSi). This initiative facilitates the

Fig. 10. The Move2THz project consortium illustrated across the value chain.

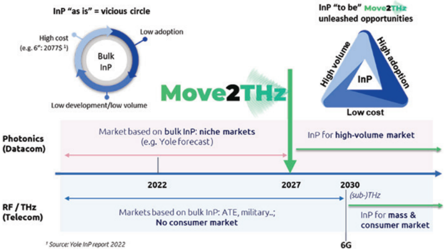

Fig. 11. The Move2THz project aims to break the current vicious cycle, enabling the adoption of InP in large-volume mass markets.

scale-up of wafer size and volume while ensuring compatibility with CMOS standards and minimizing the use of rare InP resources. By establishing a robust value chain from materials to demonstration, Move2THz aims to transform InP from a niche technology into a sustainable and commercially viable platform. This advancement will enable mass-market applications like 6G mobile communication, photonics datacom, RF/bio sensing to utilize frequencies up to THz levels. The methodology on how the Move2THz project aims to enable the adoption of InP in large-volume mass markets is illustrated in Figure 11.

The Move2THz project develops innovative PAs, LNAs, and heterogeneous integration blocks using advanced and environmentally friendly substrates and fabrication processes. These technologies will be integrated and tested for D-Band circuits, sensing, Satcom, non-terrestrial networks, as well as photonics applications.

Alternatively, to InP, RF gallium nitride (GaN) technology also demonstrates significant advantages for RF PAs in 5G base stations using GaN on silicon carbide (SiC) substrates. Soitec has developed a pioneering concept with the Smart Cut process, introducing GaN-on-X substrates that overcome the physical limitations of heteroepitaxial growth. This method involves transferring a thin GaN film onto a handling substrate (such as Si, SOI, polySiC, etc.), specifically tailored for RF applications. This innovation enables the creation of devices with superior thermal resistance, higher power density, improved power efficiency, and reduced memory effects with enhancing linearity. The new SmartGaN substrates demonstrated in 8“ diameter, address industry concerns regarding GaN quality, CMOS compatibility, thermal conductivity, and cost/availability. This SmartGaN substrate stack-up is illustrated in Figure 12. The value proposal for RF next generation of GaN devices included best-in-class PA performance for 5G and beyond, co-integration of PA and switches, and enabling frequencies beyond 70 up to 100 GHz.

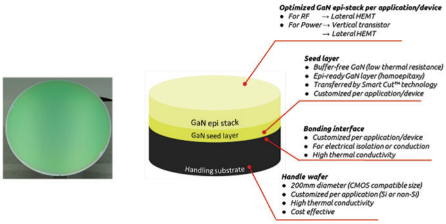

Fig. 12. The SmartGaN substrate stack-up for optimized power or RF applications.

IV. CONCLUSION

European leadership in key markets necessitates the establishment of a complete and reliable supply chain starting from material level up to applications. The industry-proven Smart Cut technology, known for its efficiency in low-power digital applications, sensing and telecommunications, can be adapted to other materials, unlocking application opportunities. By promoting the value chain model, the KDT projects BEYOND5 and Move2THz stimulate synergies and accelerate the development and adoption of new technologies, ensuring a faster time to market.

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François Brunier (Member, IEEE) graduated as physics and electronics Engineer from Centrale-Supelec in 1997. From 1998 to 2002, he worked as a device integration engineer for embedded DRAM products in STMicroelectronics Crolles. In 2002, he joined Soitec as head of advanced characterization laboratory. From 2009 to 2011, as a product manager, he led the RF-SOI and power SOI product development and offering. Since 2012, as a partnership program manager, he has been in charge of European collaborative Chips JU programs, IPCEI and public relations.