Appendix

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Presentation title: InP on Si Technologies for Next-Generation Optical Communication High-speed Analog Front-Ends

SHORT ABSTRACT OF PRESENTATION

To achieve transmission speeds exceeding 1 Tb/s per channel at low cost/bit, it is essential to generate electrical multi-level pulse-amplitude modulated signals (PAM-4/8) at extremely high symbol-rates (>100 GBaud) [1]. Current digital systems heavily rely on silicon-based digital-to-analog converters (DACs), which analog bandwidth typically caps around 30–40 GHz [2]. Consequently, their signal-to-noise ratio (SNR) is often sacrificed to digitally enhance their bandwidth. This necessitates a DAC with a high effective number of bits at half the Nyquist frequency (>3–4 typically), leading to increased footprint and power consumption of the DAC IC. Along with the silicon CMOS data converters, silicon germanium (SiGe) linear amplifiers are often used to drive the optical modulators. However, these SiGe drivers suffer from a restricted bandwidth × output swing of less than 180 GHz.Vpp [3]-[4]. As a consequence, optical transmitter front-ends are either based on (i) sub-driven high-bandwidth modulators, which restrict the link reach and/or symbol-rate due to the subsequent optical SNR penalties, or (ii) low-Vpi modulators, compromising the overall bandwidth and/or footprint depending on which technology is used. Furthermore, power hungry digital signal processing (DSP) is frequently used to address various impairments, including bandwidth limitations, which significantly increases transceivers' power consumption, the link latency, and the analog signal peak-to-average power ratio (PAPR). Higher PAPR demands higher linearity in the analog front-end, thereby affecting its power consumption. Moreover, for next-generation optical systems operating beyond 200 GBaud, severe bandwidth degradations are caused by chip-to-chip interconnections and packaging [4], requiring extra DSP for compensation.

However, InP DHBT technologies have shown a high potential to bridge this performance gap, leveraging their very-high cutoff frequencies and large output power

capabilities [5], [6]. Indeed, in [7], using InP DHBTs, the monolithic integration of an analog multiplexer (AMUX) and a linear modulator driver has demonstrated record gain-bandwidth product and output swing. This integrated circuit (IC) can aggregate two DACs bandwidth and double their sampling-rate to generate extremely high symbol-rate arbitrary signals, while directly driving the modulator. Moreover, leveraging the same technology, an electro-optical bandwidth surpassing 85 GHz has been achieved in [8], in employing an InP AMUX-driver and a thin film lithium niobate modulator. This assembly has shown 100-GBaud PAM-4 optical signals without any support of DSP. Additionally, InP DHBTs have enabled the realization of modulator driver ICs with performances exceeding 300 GHz.Vpp [9], [10]. Nonetheless, their integration onto silicon remains a challenge, to date, posing limitations on their widespread industrial adoption.

Within the Move2THz project, several paths are being explored to achieve seamless integration of InP technologies onto Si, within commercially viable frameworks. This is expected to substantially expand the opportunities for InP devices to serve as the backbone of future communication systems' analog front-ends.

During our presentation, we discuss the challenges related to the design of large-swing, high-efficiency, and extreme-high-symbol-rate analog electronics for next-generation optical communication systems offering more than 1.6 Tb/s, as well as for 6G mobile systems. Additionally, we illuminate the potential of InP-on-Si technologies to enhance signal integrity, as well as to improve thermal management and packaging.

KEYWORDS

Indium phosphide (InP), InP on silicon (InPoSi), analog multiplexer (AMUX), linear modulator driver, Tb/s optical communications, 6G, digital analog converter (DAC), digital signal processing (DSP)

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BIOGRAPHY

Romain Hersent (Member, IEEE) received the Engineering degree in electrical engineering from the ENSEA, Cergy, France, in 2016, and the Ph.D. degree in electrical engineering from L'Université de Cergy-Pontoise, Cergy, in 2020. He joined Nokia Bell Laboratories and III-V Lab, Nozay, France, in 2020, where he is currently a research engineer. His work focuses on the design and characterization of high-symbol-rate large-output-swing InP-DHBT integrated circuits for over 1 Tb/s/channel optical communications, and more specifically on analog multiplexers and linear drivers. Dr. Hersent is a member of the IEEE.