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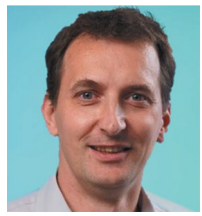

Presentation title: Post-process Substrate Porosification for RF Applications

SHORT ABSTRACT OF PRESENTATION

The issue of the interaction of free charge carriers in the substrate with RF signals propagating through passive and active devices is well known [1]. This causes signal and efficiency losses, harmonic or intermodulation distortion, and cross-talk between devices. High-porosity, micro-porous silicon has been proposed as a potential solution to this problem [2], because the lateral dimensions of the remaining inter-pore silicon can be made small enough to induce a complete depletion, resulting in some cases in an effective resistivity above 100 kOhm. cm. Therefore, porous silicon is a promising technology for applications like low-noise amplifiers or RF switches. For higher power density devices (such as power amplifiers), the thermal conductivity of porous silicon may be too low to dissipate the power of the losses.

Typically, porous silicon is formed by an electro-chemical method prior to the fabrication of the CMOS circuitry. However, porous silicon is mechanically much more fragile than bulk silicon and it has a melting point of only 800 °C. Moreover, its sponge-like 3D structure easily traps contaminants and modifies the wetting properties, leading to poor cleanability. This makes the integration with various fab processes extremely challenging.

Instead, we have already proposed a novel approach to fabricate porous silicon in a post-CMOS-process approach [3]. This low temperature process only interacts with the backside of the wafers and is thus completely independent of the front-side layout and allows for local porosification. Excellent RF performance [4], including at high temperature up to 175 °C has been demonstrated [5]. The same technique was applied "post-epitaxy" to GaN-on-Si epitaxial wafers intended for RF applications [6], achieving RF losses under 0.1 dB/mm at 5 GHz and low second harmonic distortion H2 = −140 dBm at P_{out} = 15 dBm.

These results were obtained on highly p-doped Si substrates with resistivity below 20 mOhm.cm. Such low resistivity facilitates the porosification process, as the latter is essentially governed by hole exchange at the semiconductor-electrolyte interface: low resistivity substrates allow for a more uniform hole current and as a consequence a more uniform porous silicon layer. Unfortunately, the high boron doping in these substrates causes a concern for cross-contamination and therefore such substrates are not favored for introduction into RF-CMOS fabs.

In this work, we present a wafer-level, localized post-process porosification approach on semi-standard p-type silicon substrates with resistivity levels between 1 and 20 Ohm.cm. We will describe a number of modifications to the substrate layer stack and the electrode configuration that allow for the creation of homogenous porous silicon pockets on semi-standard substrates with an industry-relevant diameter. Small- and large-signal RF characterization data of effective resistivity, harmonic distortion, intermodulation distortion, and cross-talk will be presented.

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KEYWORDS

Harmonic distortion, intermodulation distortion, porous silicon, radio frequency, mmWave

BIOGRAPHY

Joff Derluyn (Member, IEEE) was born in Roeselare, Belgium, on March 13, 1974. He received the master’s degree in electrical engineering from the University of Gent, Belgium, in 1998 and the Ph.D. degree in electrical engineering from the same institution in 2003 on the topic of epitaxy of dilute nitrides by MOCVD. He has worked at imec on the processing and characterization of GaN-based electronic devices. In 2010, he co-founded EpiGaN and served there as CTO until 2019 when EpiGaN was acquired by Soitec. At Soitec, he was a scientific director until 2022. He since joined Incize in Louvain-la-Neuve, Belgium, where he is a Fellow. He is the author of over 90 peer-reviewed papers or conference contributions and is co-inventor of 18 patent families. Dr. Derluyn’s research interests focus on the interplay between material properties and semiconductor device physics.