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# 9's Complement Encoder using QCA Schematics

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## Abstract.

Quantum Dot Cellular Automata (QCA) is an emerging technique that utilizes confinement and tunnelling of electrons and nano-scale particles to execute logical computational functions. The foundation of QCA is electron confinement in cells consisting of quantum mechanical interactions between the AlGaAs substrate within which quantum wells are formed, where the probability of an electron occurrence can be adjusted by shifting the transverse polarization applied to the cell. Digital Logic Combinational or Sequential Topologies can be realised utilising nanoscale QCA cells, this paper will demonstrate a novel method to implement a 4 bit counting operation using a Fixed Polarized Input, using 18x18 nm<sup>2</sup> cells with 4-Quantum Confinement Wells visualised as dots or holes in the software QCADesigner(2.0.3), by Walus K., which allowed us to model most Logical CMOS circuitry at ease.

**Keywords.** Coulombic Blockade, Electron Confinement, Tunnelling, Cellular Automata

## 1. INTRODUCTION

QCA cells, proposed in 1993, Lent et al.[1, 2] can be represented as a square planar structure of 18x18 nm<sup>2</sup> which has 4 quantum wells that are capable of electron confinement, and are generally doped with 2 extra electrons. Upon polarization, it is possible for the electrons to tunnel between the adjacent vertical well. This is provided via underlying clocking wires each shifted by a phase of 90°, namely Clock 0 to 3. These clocking signals essentially govern the cell configuration. The state of the cells can be classified into SHIFT, HOLD, RELEASE and RELAX, which will determine the cells mode of operation.

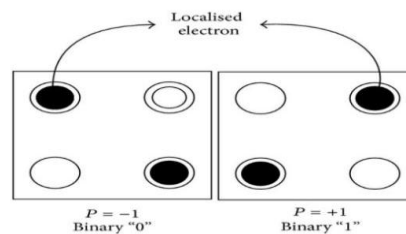


Figure 1. Two Possible polarization states which can be inferred as binary logic [1, 0]

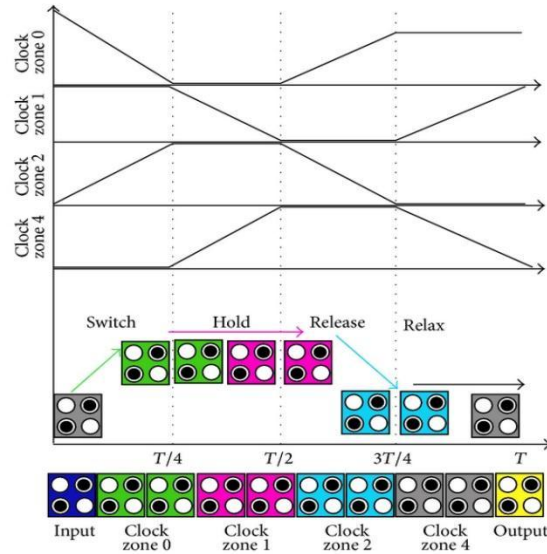


Figure 2. Clocking for Data Transmission across zones [3]

However, the ideal operating conditions of QCA based implementations is to isolate the system from any external energy by keeping the temperatures as low as 4-10 K to keep the Kink Energy[4] between the cells minimal for an ideal adiabatic switching of QCA cells which is essential for their intended applications and advantages over any other computing systems, as it enables data transmission without any actual flow of current [5] making it extremely efficient when working at clocking speeds in the range of Tera-Hertz switching speeds, with nearly negligible energy dissipation.[6], [7] .

## 2. LOGICAL DESIGN AND QCA IMPLEMENTATION

Following the general design of a 9's complement converter, with 4 input and output cells designated in the schematic. A basic logic circuit would include a 4-bit BCD [8]–[10] input labelled accordingly as  $A_0$ ,  $A_1$ ,  $A_2$  and  $A_3$ . Similarly, the output cells were indexed with  $Y$  from 0-3. A simple logic circuit is presented in Fig 3, upon which the final QCA schematic is based upon.

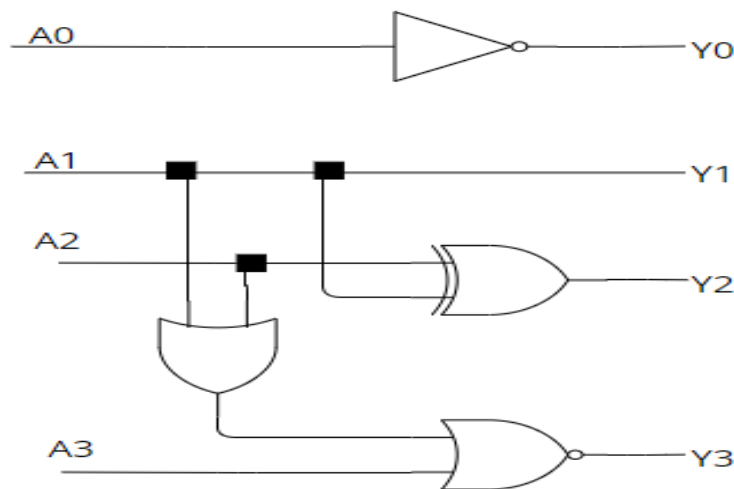


Figure 3. The Generic Logic Structure of a 9s Complement Converter

A Binary Coded Decimal Digit's 9's Complement would classify as the BCD that would result in a decimal value of 9 when added. This principle of conversion yields positive results for the BCD < 9, else would result in a negative signed number.

TABLE 1. TRUTH TABLE FOR INPUT AND ITS 9'S COMPLEMENT VALUES

BCD	4-bit Binary Equivalent				9's Comp	4-bit Binary Equivalent			
0	0	0	0	0	9	1	0	0	1
1	0	0	0	1	8	1	0	0	0
2	0	0	1	0	7	0	1	1	1
3	0	0	1	1	6	0	1	1	0
4	0	1	0	0	5	0	1	0	1
5	0	1	0	1	4	0	1	0	0
6	0	1	1	0	3	0	0	1	1
7	0	1	1	1	2	0	0	1	0
8	1	0	0	0	1	0	0	0	1
9	1	0	0	1	0	0	0	0	0

In order to establish the relation between the Inputs and the Outputs in a QCA structure, the logic gates were established using majority gates [11] and inverter gates. Redundant cells were removed and Clocking zones were optimised for an ideal performance of the Converter.

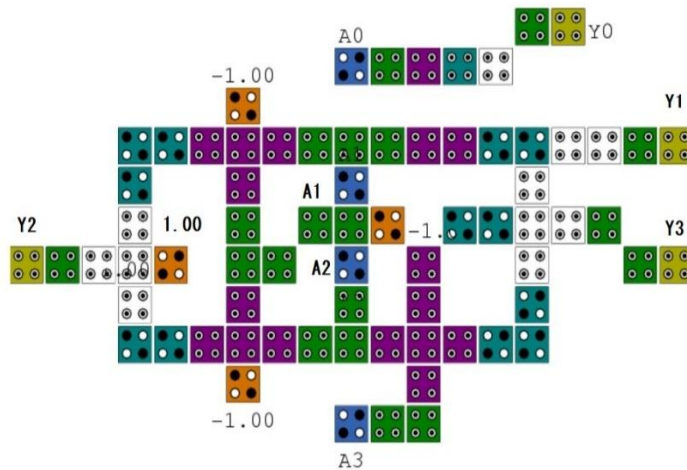


Figure 4. Proposed Schematic of a 9's complement BCD encoder

The depicted circuit shows an equivalent logic circuit in a QCA domain where the input BCD in its binary representation is converted to its 9's complement, which is useful in subtraction/addition of higher bit numbers with ease. Especially in the case of Signed Subtraction Methods. This circuit adds to the plethora of designs that are available as design analogies for CMOS to QCA migration. However, fabrication challenges are still well beyond our present limits for an idealised operation.

## 2.1. Simulation Results

The outputs are obtained via the bistable approximation engine, with the QCA Designer allows changing the number of recorded samples by increasing the number of iterations. Same can be done for the Clock Zone frequency by using various arrangements of the clocking wires underneath the main cell, however, there will be a proposed maximum limit of switching frequency due to presence of Quantum Coherence between the cells, the exact value of the limit is dependent on the area of the design and the number of cells used.



Figure 6. Converted Outputs as Simulation Results

The resultant output clearly demonstrates that the conversion of BCD encoding can be further realized for the creation of a robust ALU block made of purely QCA cells, capable of handling much higher bit operations at a scale of almost Terahertz speeds of processing.

## 3. REFERENCES

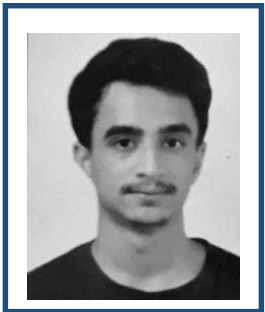
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## Biographies



Sristi Chakraborty is currently the BTech student of Computer Science and Engineering (Data Science) at Techno Main Salt Lake under Maulana Abul Kalam Azad University of Technology, West Bengal, India.



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